Evaluation board with STM32L552ZE MCU

Introduction

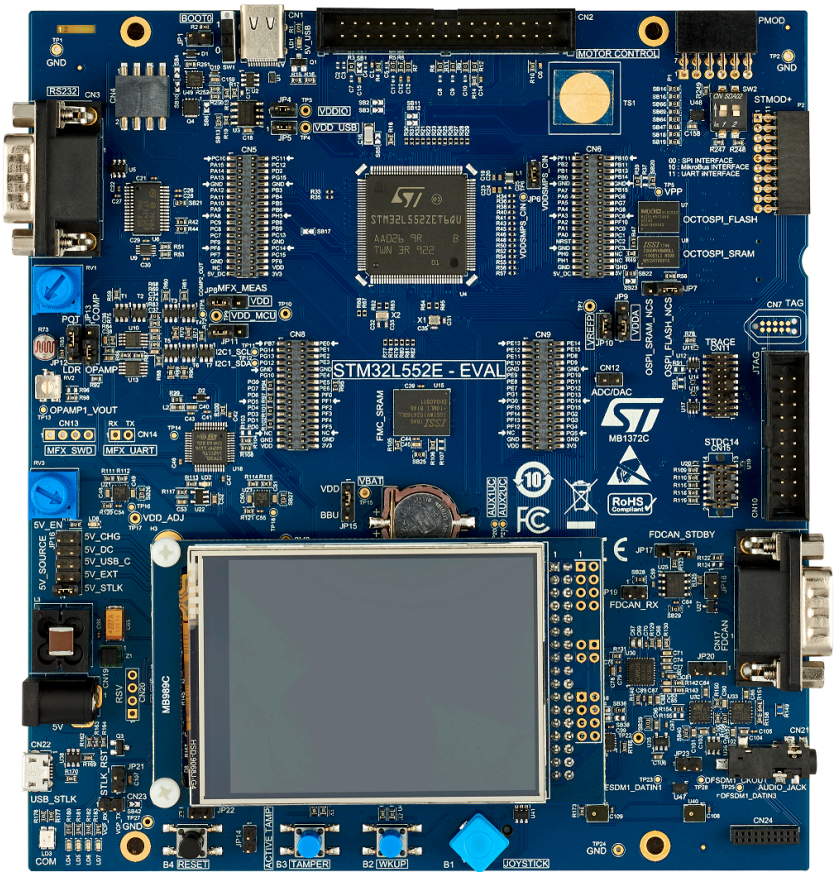
The STM32L552E-EV Evaluation board is designed as a complete demonstration and development platform for STMicroelectronics Arm® Cortex®-M33 core with Arm® TrustZone® and the ARMv8-M mainline security extension.

The STM32L552E-EV Evaluation board is based on an ultra-low-power STM32L552ZET6QU microcontroller with 512 Kbytes of Flash memory and 256 Kbytes of SRAM, one external memory interface supporting an LCD interface, one Octo-SPI memory interface, one USB Type-C™ FS with Power Delivery controller, two SAI ports, four I²C buses, six USART ports, three SPI interfaces, one CAN-FD controller, one SDMMC interface, 2 × 12-bit ADC, 2 × 12-bit DAC, two operational amplifiers, two ultra-low comparators, four digital filters for sigma-delta modulator, up to 16 timers, touch-sensing capability, and debugging supported by SWD, JTAG and ETM interface.

The full range of hardware features on the board helps the user to evaluate all the peripherals (USB FS, USART, digital microphones, ADC and DAC, dot-matrix TFT LCD, LDR, SRAM, octal Flash memory device, microSD™ card, sigma-delta modulators, smartcard, CAN-FD transceiver, I²C, EEPROM), and to develop applications. Extension headers allow easy connection of a daughterboard or wrapping board for a specific application.

An ST-LINK/V2-1 is integrated on the board, as embedded in-circuit debugger and programmer for the STM32 MCU and the USB Virtual COM port bridge.

Figure 1. STM32L552E-EV Evaluation board (top view)



Picture is not contractual.

1 Features

- STM32L552ZET6QU microcontroller featuring 512 Kbytes of Flash memory and 256 Kbytes of SRAM in LQFP144 package
- 2.8" 240 × 320 pixel-262K color TFT LCD module with parallel interface and touch panel
- USB Type-C™ Sink device FS
- On-board current measurement
- SAI Audio CODEC
- ST-MEMS digital microphones
- 512-Mbit Octal-SPI Flash, 64-Mbit Octal HyperRAM, 16-Mbit SRAM, 128-Kbit I^2C EEPROM
- 4 user LEDs
- User, Tamper and Reset push-buttons
- 4-direction joystick with a selection button
- 1 touch sensing button
- Light-dependent resistor (LDR)
- Potentiometer
- Coin-battery cell holder for power backup
- Power-metering demonstration with dual-channel, sigma-delta modulator
- Board connectors:
  - Power jack
  - USB Type-C™
  - microSD™ card
  - Smartcard socket
  - Stereo headset jack including analog microphone input
  - Audio jack for external speakers
  - 2× DB9 for external RS-232 port and CAN FD
  - JTAG and ETM trace debugger
  - Connectors for ADC input and DAC output
  - I/O expansion connectors
  - STMod+ expansion connector
  - Pmod™ expansion connector
  - Audio daughterboard expansion connector
  - Motor-control interface expansion connector
  - I^2C expansion connector
- Flexible power-supply options: ST-LINK, USB V_{BUS} or external sources
- On-board ST-LINK/V2-1 debugger/programmer with USB re-enumeration capability: mass storage, Virtual COM port, and debug port
- Comprehensive free software libraries and examples available with the STM32CubeL5 MCU Package
- Support of a wide choice of Integrated Development Environments (IDEs) including IAR™, Keil®, and STM32CubeIDE

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Ordering information

To order the STM32L552E-EV Evaluation board, refer to Table 1. Additional information is available from the datasheet and reference manual of the target STM32.

Table 1. Ordering information

Order code	Board references	Target STM32
STM32L552E-EV	• MB1372 • MB989(1)	STM32L552ZET6QU

1. *LCD board.*

2.1 Product marking

Evaluation tools marked as “ES” or “E” are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

“E” or “ES” marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet “Package information” paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

In order to use the same commercial stack in his application, a developer may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

2.2 Codification

The meaning of the codification is explained in Table 2. The order code is mentioned on a sticker placed on the top side of the board.

Table 2. Codification explanation

STM32TTXXY-EV	Description	Example: STM32L552E-EV
STM32TT	MCU series in STM32 32-bit Arm Cortex MCUs	STM32L5 Series
XX	MCU product line in the series	STM32L552
Y	STM32 Flash memory size: • E for 512 Kbytes	512 Kbytes

3 Development environment

3.1 System requirements

- Windows® OS (7, 8 and 10), Linux® 64-bit, or macOS®
- USB Type-A to Micro-B cable

Note: macOS® is a trademark of Apple Inc. registered in the U.S. and other countries.
All other trademarks are the property of their respective owners.

3.2 Development toolchains

- IAR™ - EWARM (see note)
- Keil® - MDK-ARM (see note)
- STMicroelectronics - STM32CubeIDE

Note: On Windows® only.

3.3 Demonstration software

The demonstration software, included in the STM32Cube MCU Package corresponding to the on-board microcontroller, is preloaded in the STM32 Flash memory for easy demonstration of the device peripherals in standalone mode. The latest versions of the demonstration source code and associated documentation can be downloaded from *www.st.com*.

4 Conventions

Table 3 provides the conventions used for the ON and OFF settings in the present document.

Table 3. ON/OFF convention

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper should be fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered

5 Delivery recommendations

Before the first use, make sure that no damage occurred to the board during shipment and no socketed components are loosened in their sockets or fallen into the plastic bag. In particular, pay attention to the following components:

1. microSD™ card is in its CN25 receptacle.
2. LCD module MB989 daughterboard is in its CN18 connector, and LCD screw, spacer, and nut are in place.

For product information related to the STM32L552ZET6QU microcontroller, visit *www.st.com* website.

6 Hardware layout and configuration

The STM32L552E-EV Evaluation board is designed around the STM32L552ZET6QU target microcontroller. Figure 2 illustrates STM32L552ZET6QU connections with peripheral components. Figure 3 shows the location of the main components on the top side of the Evaluation board, and Figure 4 shows the location of the main components on the bottom side of the Evaluation board.

Figure 2. Hardware block diagram

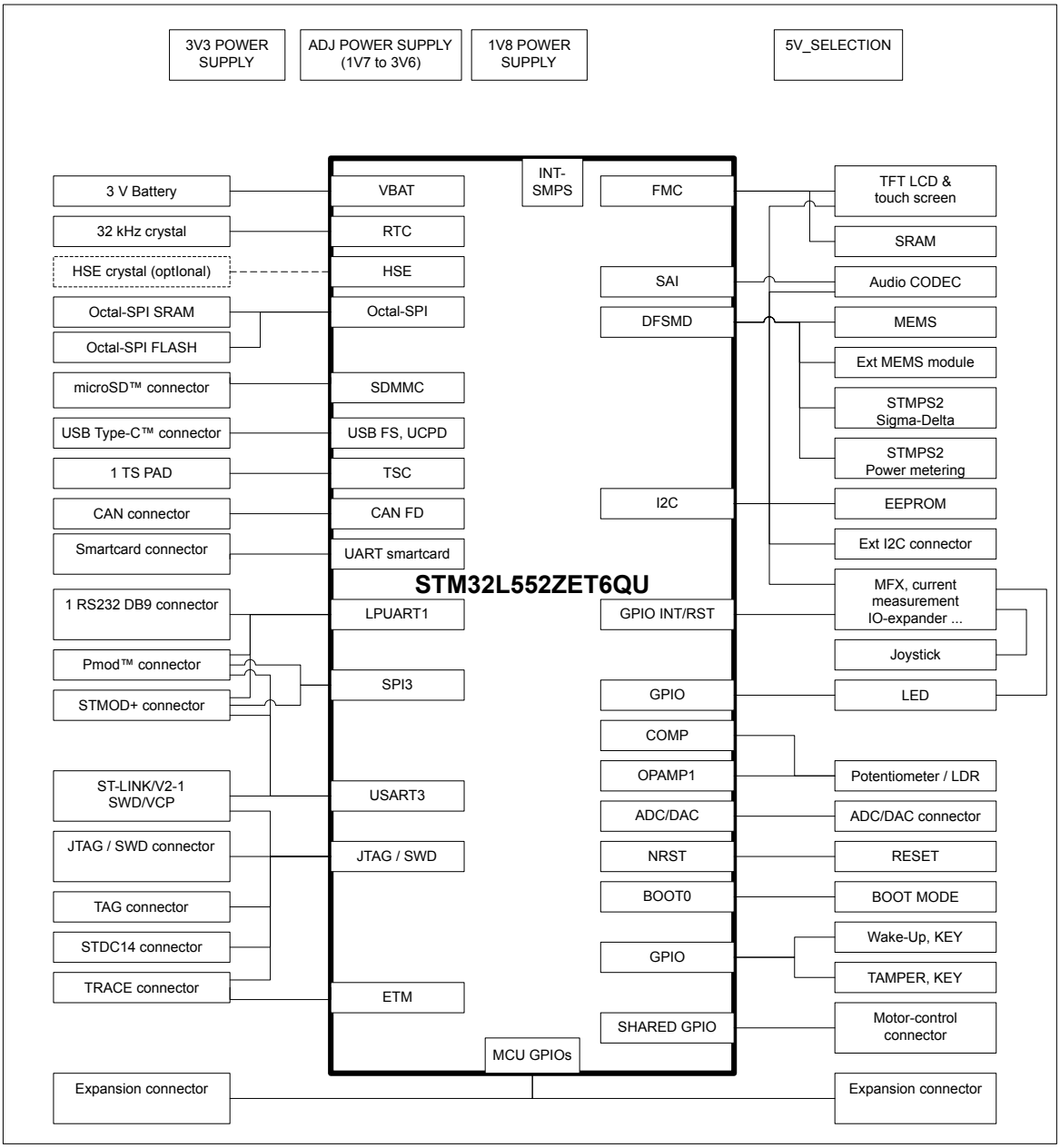


Figure 3. STM32L552E-EV PCB layout (top view)

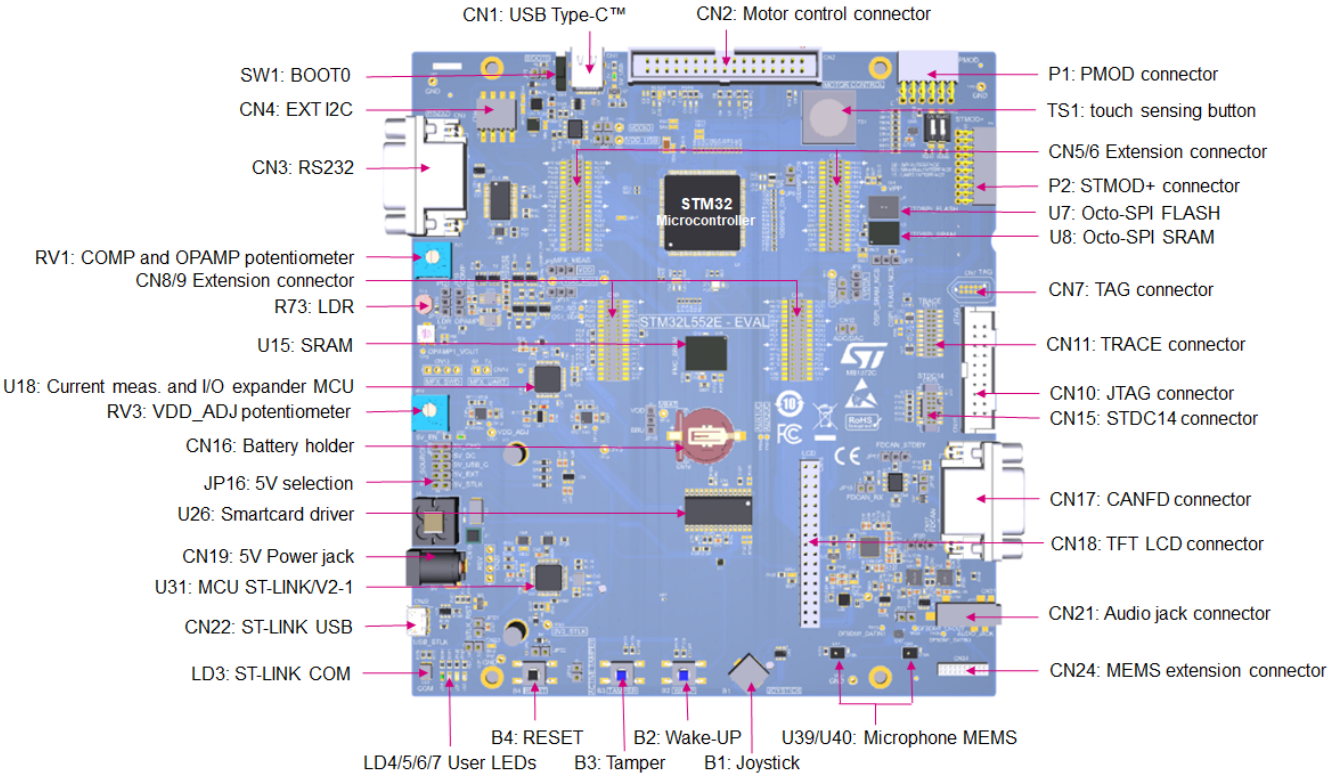
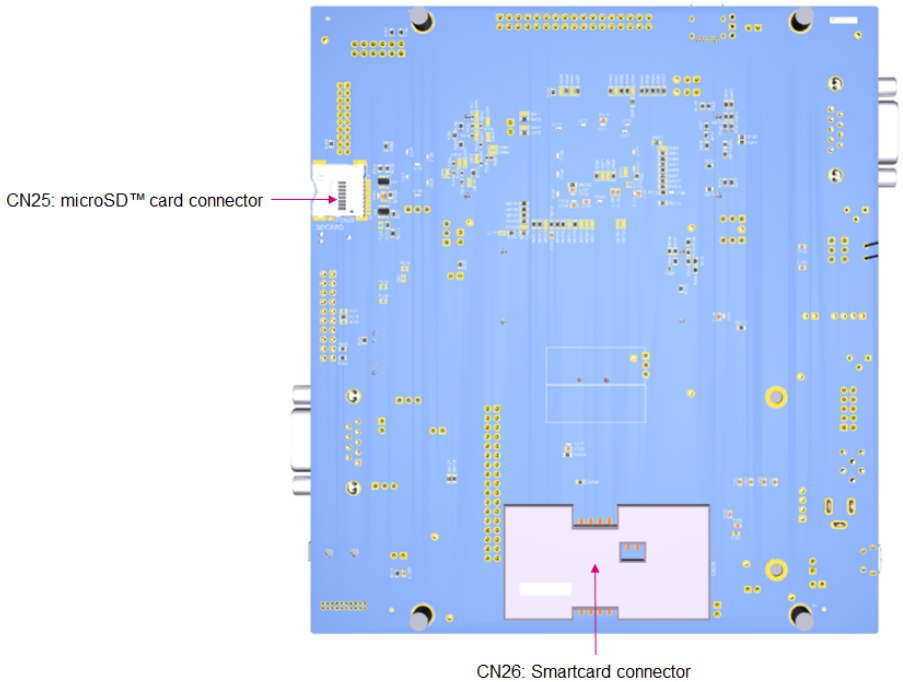


Figure 4. STM32L552E-EV PCB layout (bottom view)



6.1 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 facility for debugging and flashing of STM32L552ZET6QU is integrated on the STM32L552E-EV Evaluation board.

Compared to the ST-LINK/V2 stand-alone tool available from STMicroelectronics, ST-LINK/V2-1 offers new features and drops some others.

New features:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

Features dropped;

- SWIM interface

The CN22 USB connector can be used to power STM32L552E-EV regardless of the ST-LINK/V2-1 facility used for debugging or for flashing STM32L552ZET6QU.

This holds also when the ST-LINK/V2 standalone tool is connected to CN7 TAG connector, CN10 JTAG connector, CN11 TRACE connector or CN15 STDC14 connector and used for debugging or flashing STM32L552ZET6QU. Section 6.6 Power supply provides more detail on powering STM32L552E-EV.

For full detail on both versions of the debugging and flashing tool, the stand-alone ST-LINK/V2 and the embedded ST-LINK/V2-1, refer to *www.st.com*.

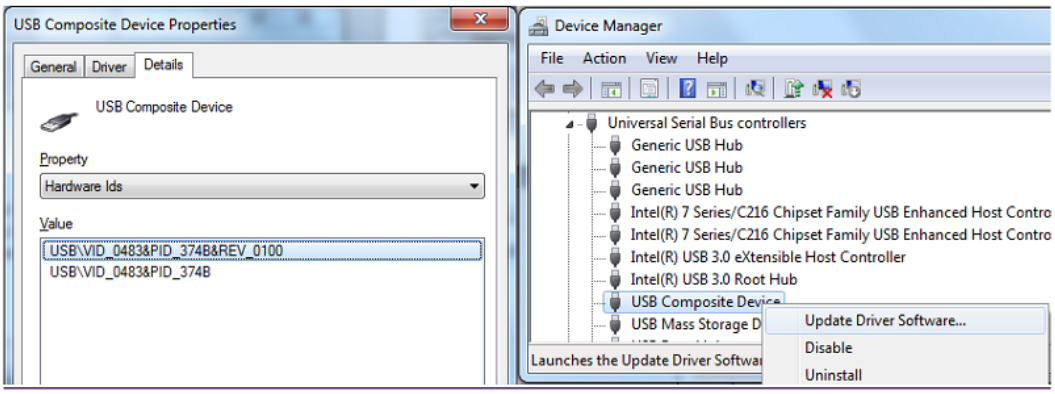
6.1.1 Drivers

The ST-LINK/V2-1 requires a dedicated USB driver, which, for Windows 7®, Windows 8® and Windows 10®, is found at *www.st.com*.

In case the STM32L552E-EV board is connected to the PC before the driver is installed, some STM32L552E-EV interfaces may be declared as *"Unknown"* in the PC device manager. In this case, the user must install the dedicated driver files, and update the driver of the connected device from the device manager as shown in Figure 5.

Note: Prefer using the USB Composite Device handle for a full recovery.

Figure 5. USB composite device



6.1.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware mechanism for the in-situ upgrade through the USB port. As the firmware may evolve during the lifetime of the ST-LINK/V2-1 product (for example new functionalities, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32L552E-EV board and periodically, to stay up-to-date with the latest firmware version.

6.2 ETM trace

CN11 connector, header 10x2-pin 1.27 mm pitch, can output trace signals used to debug.
Table 4 describes the HW configuration for the TRACE function.

Table 4. HW configuration for the CN11 TRACE connector

I/O	Bridge	Setting(1)	Comment
PC9	SB59	**ON**	**PC9 can be used for the TRACE function TRACE D0.**
		OFF	PC9 is not connected to TRACE. PC9 can be used for SDIO.
PC10	SB68	**ON**	**PC10 can be used for the TRACE function TRACE D1.**
		OFF	PC10 is not connected to TRACE. PC10 can be used for SDIO.
PC12	SB53	**ON**	**PC12 can be used for the TRACE function TRACE D3.**
		OFF	PC12 is not connected to TRACE. PC12 can be used for SDIO or STMOD+.
PE2	R230	**ON**	**PE2 can be used for the TRACE function TRACE CLK.**
		OFF	PE2 is not connected to TRACE. No other muxing
PE5	R95	**ON**	**PE5 can be used for the TRACE function TRACE D2.**
		OFF	PE5 is not connected to TRACE. No other muxing

1. *The default configuration is shown in bold.*

Figure 6 shows the TRACE connector pinout.

Figure 6. CN11 TRACE connector pinout

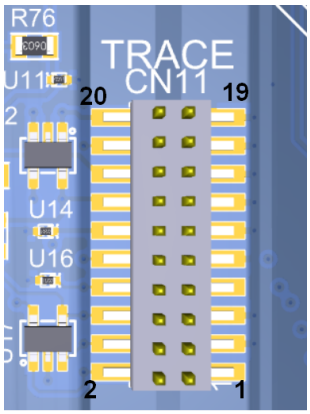


Table 5 describes the TRACE connector pinout.

Table 5. CN11 TRACE connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	2	TMS / SWDIO	PA13

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
GND	Power	3	4	TCK / SWCLK	PA14
GND	Power	5	6	TDO / SWO	PB3
-	KEY	7	8	TDI	PA15
GND	Power	9	10	HOST NRST	NRST
GND	Power	11	12	TRACE CLK	PE2
GND	Power	13	14	TRACE D0	PC9
GND	Power	15	16	TRACE D1	PC10
GND	Power	17	18	TRACE D2	PE5
GND	Power	19	20	TRACE D3	PC12

6.2.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the TRACE features:

The TRACE function cannot be operated simultaneously with the SDCARD function.

The TRACE function cannot be operated simultaneously with the STMOD+ (SPI) function.

6.3 JTAG connector

The connector CN10, header 10x2-pin 2.54 mm pitch, can output JTAG signals used to debug.

Table 6 describes the HW configuration for the JTAG function.

Table 6. HW configuration for the JTAG function on CN10 connector

I/O	Bridge	Setting[1]	Comment
PB4	SB93	**ON**	**PB4 is connected to JTAG JTRSTN.**
		OFF	PB4 is NOT connected to JTAG. PB4 can be used for COMP or STMOD+.
PA15	SB72	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is NOT connected to JTAG. PA15 can be used for UCPB.
PA13	R192	**ON**	**PA13 is connected to JTAG as JTMS or SWDIO.**
		OFF	PA13 is NOT connected to JTAG or SWD. No other muxing
PA14	R193	**ON**	**PA14 is connected to JTAG as JTCK or SWCLK.**
		OFF	PA14 is NOT connected to JTAG or SWD. No other muxing
PB3	R197	**ON**	**PB3 is connected to JTAG as JTDO (SWO).**
		OFF	PB3 is NOT connected to JTAG or SWD. PB3 can be used for the green LED.
NRST	-	-	**NRST is used to reset the target.**

1. *The default configuration is shown in bold.*

Figure 7 shows the CN10 JTAG connector pinout.

Figure 7. CN10 JTAG connector pinout

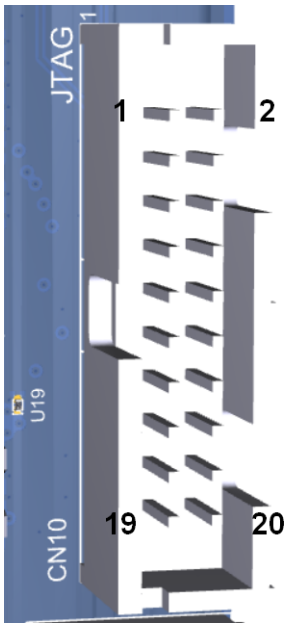


Table 7 describes the JTAG connector pinout.

Table 7. CN10 JTAG connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	2	Power	VDD
PB4	JTRSTN	3	4	Power	GND
PA15	TDI	5	6	Power	GND
PA13	TMS/SWDIO	7	8	Power	GND
PA14	TCK/SWCLK	9	10	Power	GND
-	Pull Down	11	12	Power	GND
PB3	TDO/SWO	13	14	Power	GND
NRST	Host NRST	15	16	Power	GND
-	TRGIN	17	18	Power	GND
-	TRGOUT	19	20	Power	GND

6.3.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the JTAG features:

The JTAG function is mainly limited to the SWD function, the TDI and TDO functions are optional.

The full JTAG function cannot be operated simultaneously with the COMP function.

The full JTAG function cannot be operated simultaneously with the STMOD+ function.

The full JTAG function cannot be operated simultaneously with the UCPD function.

The full JTAG function cannot be operated simultaneously with the green LED function.

6.4 STDC14 connector

The CN15 connector, header 7x2-pin 1.27 mm pitch, can also output JTAG signals used for debug compatible with STDC14.

Table 8 describes the HW configuration for the STDC14 function.

Table 8. HW configuration for the CN15 STDC14 connector

I/O	Bridge	Setting[1]	Comment
PA15	SB72	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is NOT connected to JTAG. PA15 can be used for UCPD.
PA13	R192	**ON**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
		OFF	PA13 is NOT connected to JTAG or SWD. No other muxing
PA14	R193	**ON**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
		OFF	PA14 is NOT connected to JTAG or SWD. No other muxing
PB3	R197	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is NOT connected to JTAG or SWD. PB3 can be used for the green LED.
NRST	-	-	**NRST is used to reset the target.**
PB10	SB78	**ON**	**PB10 USART3_TX is connected to T_VCP_TX.** **SB48 and SB77 must be not fitted.**
		OFF	PB10 USART3_TX is NOT connected to T_VCP_TX. PB10 can be used for RS-232 or STMOD+.
PB11	SB75	**ON**	**PB11 USART3_RX is connected to T_VCP_RX.** **SB50 and SB71 must be not fitted.**
		OFF	PB11 USART3_RX is NOT connected to T_VCP_RX. PB11 can be used for RS-232 or STMOD+.

1. *The default configuration is shown in bold.*

Figure 8 shows the CN15 STDC14 connector pinout.

Figure 8. CN15 STDC14 connector pinout

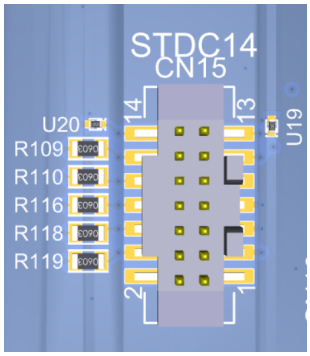


Table 9 describes the STDC14 connector pinout.

Table 9. STDC14 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
-	NC	1	2	NC	-
VDD	Power	3	4	TMS_SWDIO	PA13
GND	Power	5	6	TCK_SWCLK	PA14
GND	Power	7	8	TDO_SWO	PB3
-	KEY	9	10	TDI	PA15
-	GNDDetect: Pull-down	11	12	HOST_NRST	NRST
PB11	T_VCP_RX	13	14	T_VCP_TX	PB10

6.4.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the STDC14 features:

The JTAG function is mainly limited to the SWD function, the TDI and TDO functions are optional.

The full JTAG cannot be operated simultaneously with the COMP function.

The full JTAG cannot be operated simultaneously with the STMOD+ function.

The full JTAG cannot be operated simultaneously with the UCPD function.

The full JTAG cannot be operated simultaneously with the green LED function.

6.5 TAG footprint

The CN7 footprint can also output a debug interface compatible with the TAG probe TC2050-IDC-NL.
Table 10 describes the HW configuration for the TAG function.

Table 10. HW configuration for the CN7 TAG connector

I/O	Bridge	Setting[1]	Comment
PA15	SB72	**ON**	**PA15 is connected to JTAG JTDI.**
		OFF	PA15 is NOT connected to JTAG. PA15 can be used for UCPD.
PA13	R192	**ON**	**PA13 is connected to JTAG JTMS or SWD SWDIO.**
		OFF	PA13 is NOT connected to JTAG or SWD. No other muxing
PA14	R193	**ON**	**PA14 is connected to JTAG JTCK or SWD SWCLK.**
		OFF	PA14 is NOT connected to JTAG or SWD. No other muxing
PB3	R197	**ON**	**PB3 is connected to JTAG JTDO or SWD SWO.**
		OFF	PB3 is NOT connected to JTAG or SWD. PB3 can be used for the green LED.
PB4	SB93	**ON**	**PB4 is connected to JTAG JTRSTN.**
		OFF	PB4 is NOT connected to JTAG. PB10 can be used for COMP or STMOD+.
NRST	-	-	**NRST is used to RESET the target.**

1. *The default configuration is shown in bold.*

Figure 9 shows the TAG connector pinout.

Figure 9. CN7 TAG connector pinout

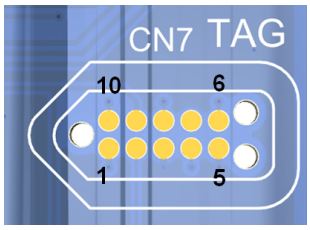


Table 11 describes the CN7 TAG connector pinout.

Table 11. CN7 TAG connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
VDD	Power	1	10	HOST NRST	NRST
PA13	TMS_SWDIO	2	9	JTAG_NRST	PB4
GND	Power	3	8	TDI	PA15
PA14	TCK_SWCLK	4	7	NC	-
GND	Power	5	6	TDO_SWO	PB3

6.5.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the TAG features:

The JTAG is mainly limited to SWD function, TDI and TDO are optional.

The full JTAG cannot be operated simultaneously with COMP function.

The full JTAG cannot be operated simultaneously with STMOD+ function.

The full JTAG cannot be operated simultaneously with UCPD function.

The full JTAG cannot be operated simultaneously with the green LED function.

6.6 Power supply

6.6.1 5 V power supply general view

The STM32L552E-EV Evaluation board is designed to be powered from 5 V DC power source. It incorporates a precise polymer Zener diode (Poly-Zen) protecting the board from damage due to the wrong power supply. One of the following five 5 V DC power inputs can be used, upon an appropriate board configuration:

- 5V_STLK from CN22 micro-B USB receptacle of ST-LINK/V2-1 (default)
- 5V_EXT from CN19 Power jack marked 5V on the board. The positive pole is on the center pin as illustrated in Figure 12.
- 5V_USB_C from CN1 USB Type-C™ receptacle of USB user interface
- 5V_DC from pin 37 of CN5 or Pin 37 of CN6 extension connectors for the custom daughterboard
- 5V_CHG from CN22 Micro-B USB receptacle of ST-LINK/V2-1, in case of wall charger (no-enumeration)

No external power supply is provided with the board.

When 5V_EXT, 5V_DC is used to power the board, this power source must comply with the standard EN-60950-1: 2006+A11/2009 and must be Safety Extra Low Voltage (SELV) with limited power capability

LD8 Green LED turns on when the voltage on the power line marked as 5V is present. All supply lines required for the operation of the components on STM32L552E-EV are derived from that 5V line.

Table 12 describes the 5V power supply capabilities.

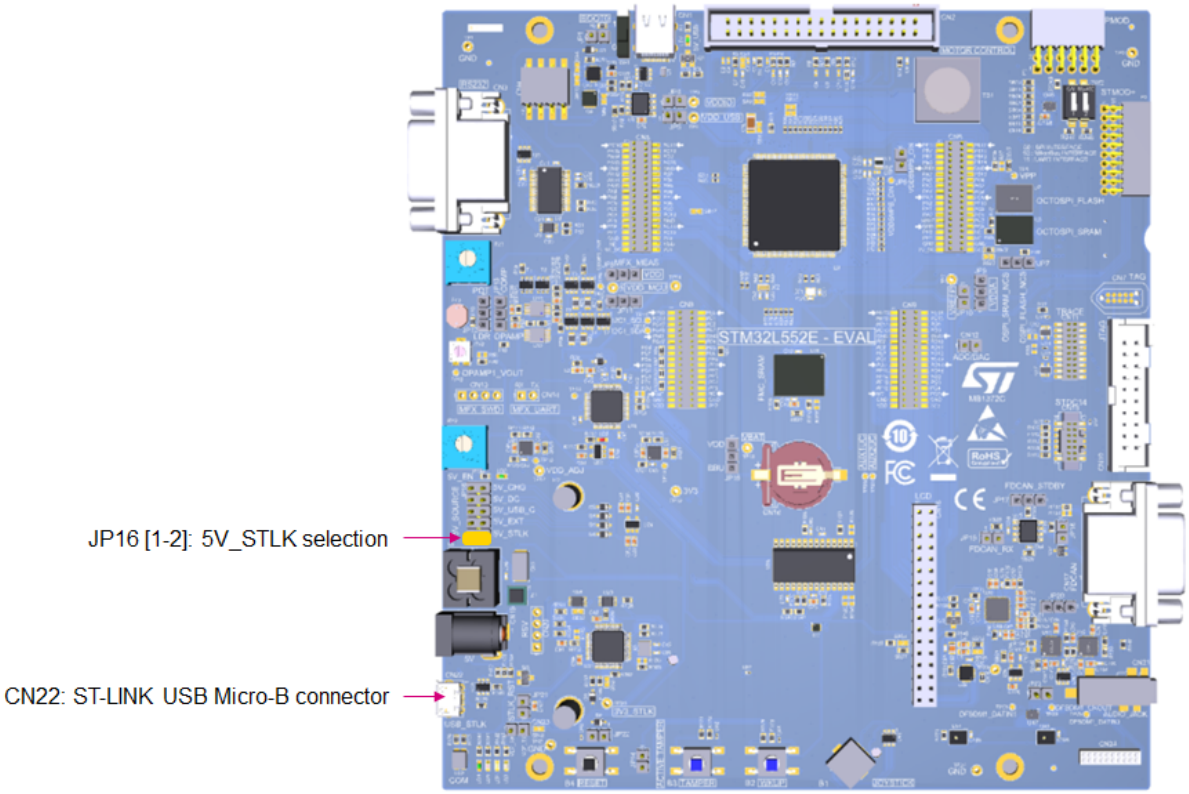
Table 12. Power supply capabilities

Input Power name	Connector pins	Voltage range	Max. current	Limitation
5V_STLK	CN22 pin 1 JP16 [1-2]	4.75 to 5.25 V	500 mA	The maximum current depends on the USB enumeration: • 100 mA without enumeration • 500 mA with correct enumeration
5V_EXT	C19 pin 1 JP16 [3-4]		-	-
5V_USB_C	CN1 JP16 [5-6]		1 A	The maximum current depends on the USB Type-C™ host used to power the STM32L552E-EV board.
5V_DC	CN5 pin37 CN6 pin 37 JP16 [7-8]		-	The maximum current depends on the power source.
5V_CHG	CN22 pin 1 JP16 [9-10]		-	The maximum current depends on the USB wall charger used to power the board (no enumeration, no current protection).

6.6.2 5V_ST_LINK power source

5V_ST_LINK is a DC power with limitation from ST-LINK USB connector (USB type Micro-B connector of ST-LINK/V2-1). In this case, the JP16 jumper must be on pin [1-2] to select the 5V_STLK power source on JP16 silkscreen. This is the default setting. If the USB enumeration succeeds, the 5V_STLK power is enabled, by asserting the PWR_ENn signal (from STM32F103CBT6). This pin is connected to a power switch STMPS2141STR, which powers the board. This power switch features also a 500 mA current limitation to protect the PC in case of an onboard short-circuit. The STM32L552E-EV board, with its shield on it, can be powered from the CN22 ST-LINK USB connector, but only the ST-LINK circuit has the power before USB enumeration, as the host PC only provides 100 mA to the board at that time. During the USB enumeration, the STM32L552E-EV board asks for the 500 mA power to the host PC. If the host is able to provide the required power, the enumeration finishes by a *SetConfiguration* command and then, the power switch is switched ON, the green LED LD8 (5V) turned ON, thus the STM32L552E-EV board and its shield on it can consume 500 mA current, but no more. If the host is not able to provide the requested current, the enumeration fails. Therefore the power switch remains OFF and the MCU part, including the extension board, is not powered. As a consequence, the green LED LD8 (5V) remains turned OFF. In this case, it is mandatory to use an external power supply. 5V_STLK power source configuration for the jumper JP16 [1-2] is described in Figure 10.

Figure 10. JP16 [1-2]: 5V_STLK PWR SOURCE



6.6.3 5V_EXT power source

5V_EXT is the DC power coming from the CN19 power jack. In this case, the JP16 jumper must be on pin [3-4] to select the 5V_EXT power source on JP16 silkscreen. The positive pole is on the center pin as illustrated in Figure 12.

5V_EXT power source configuration for jumper JP16[3-4] is described in Figure 11.

Figure 11. JP16 [3-4]: 5V_EXT PWR SOURCE

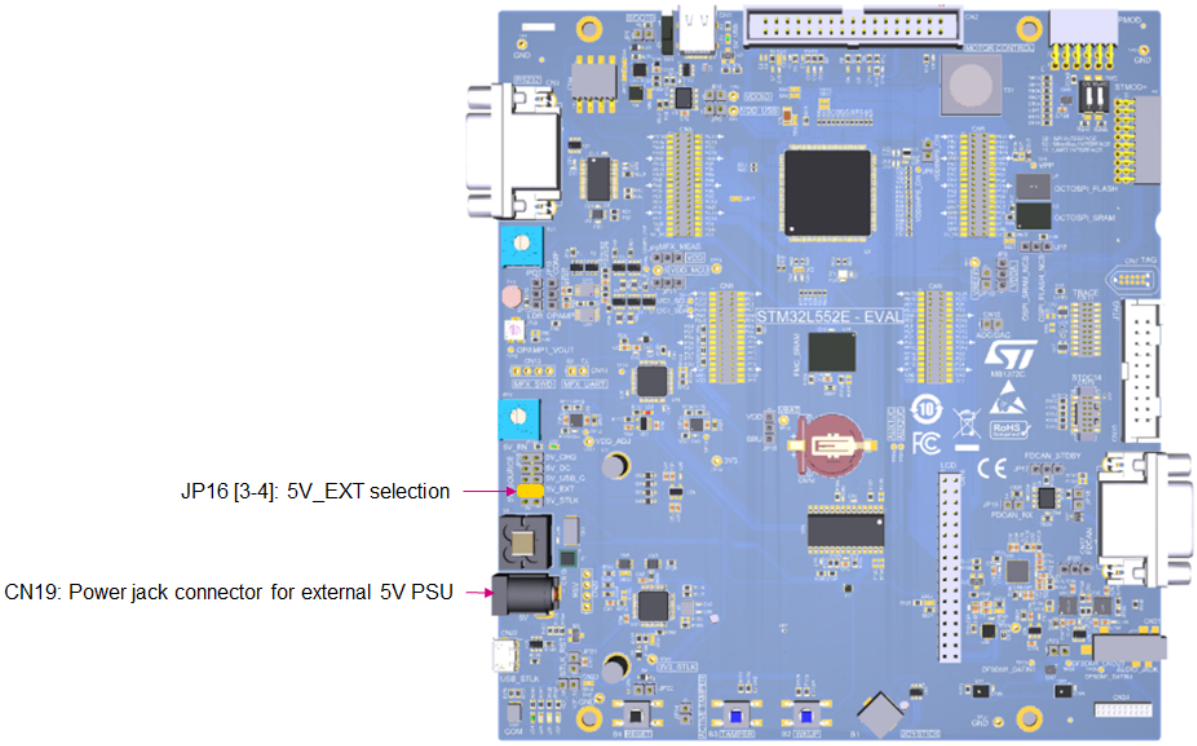
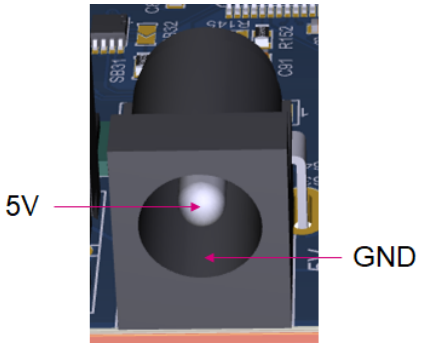


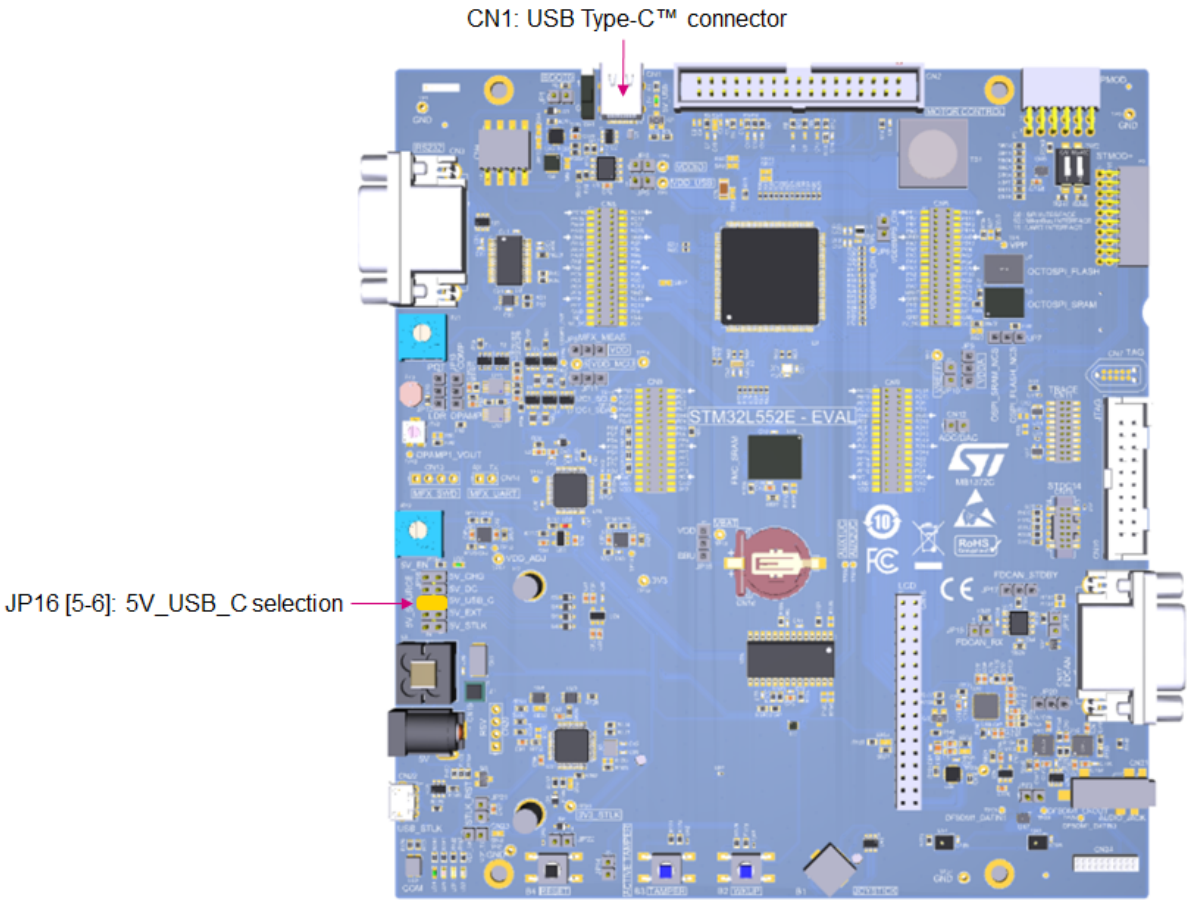
Figure 12. CN19 5V power supply connector



6.6.4 5V_USB_C power source

5V_USB_C is the DC power supply connected to the CN1 user USB Type-C™. To select the 5V_USB_C power source on JP16 silkscreen, the jumper of JP16 must be on pins [5-6]. In this case. 5V_USB_C power source configuration for jumper JP16 [5-6] is described in Figure 13.

Figure 13. JP16 [5-6]: CN1 5V_USB_C

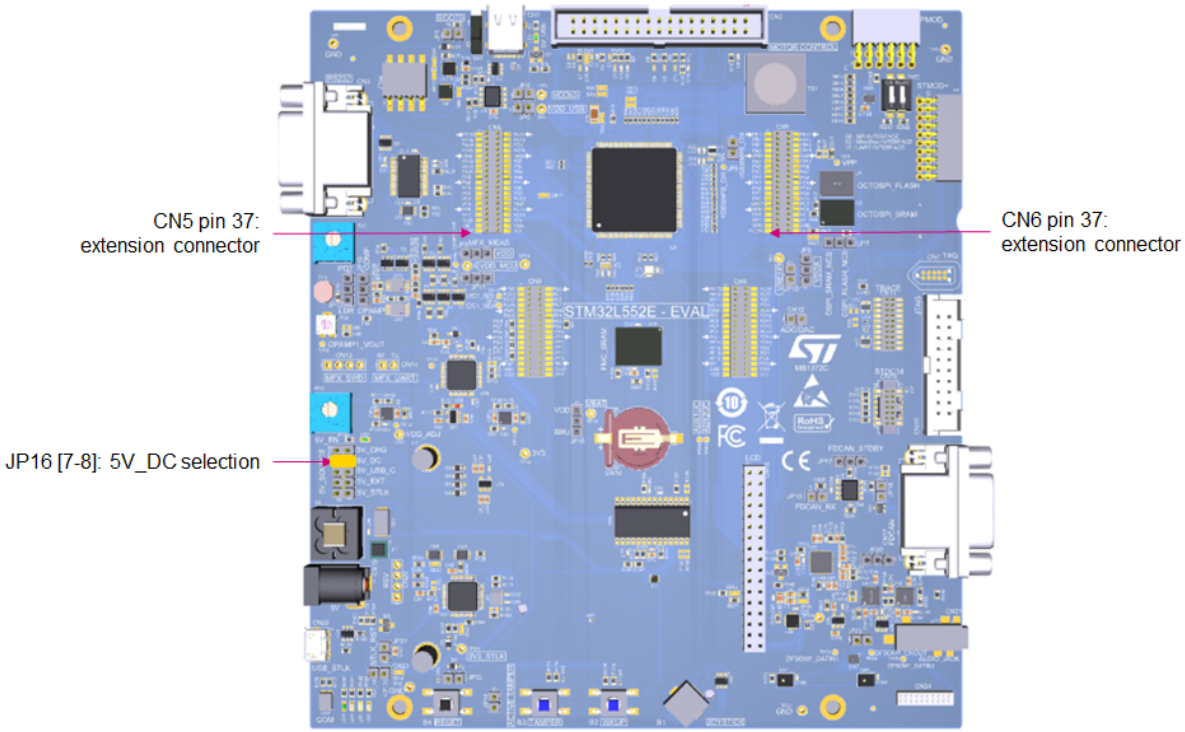


6.6.5 5V_DC power source

5V_DC is the DC power coming from external (5V DC power from CN5 pin 37 or CN6 pin 37 extension connectors. In this case, the JP16 jumper must be on pin [7-8] to select the 5V_DC power source on JP16 silkscreen.

5V_DC power source configuration for jumper JP16 [7-8] is described in Figure 14.

Figure 14. JP16 [7-8]: 5V_DC PWR SOURCE

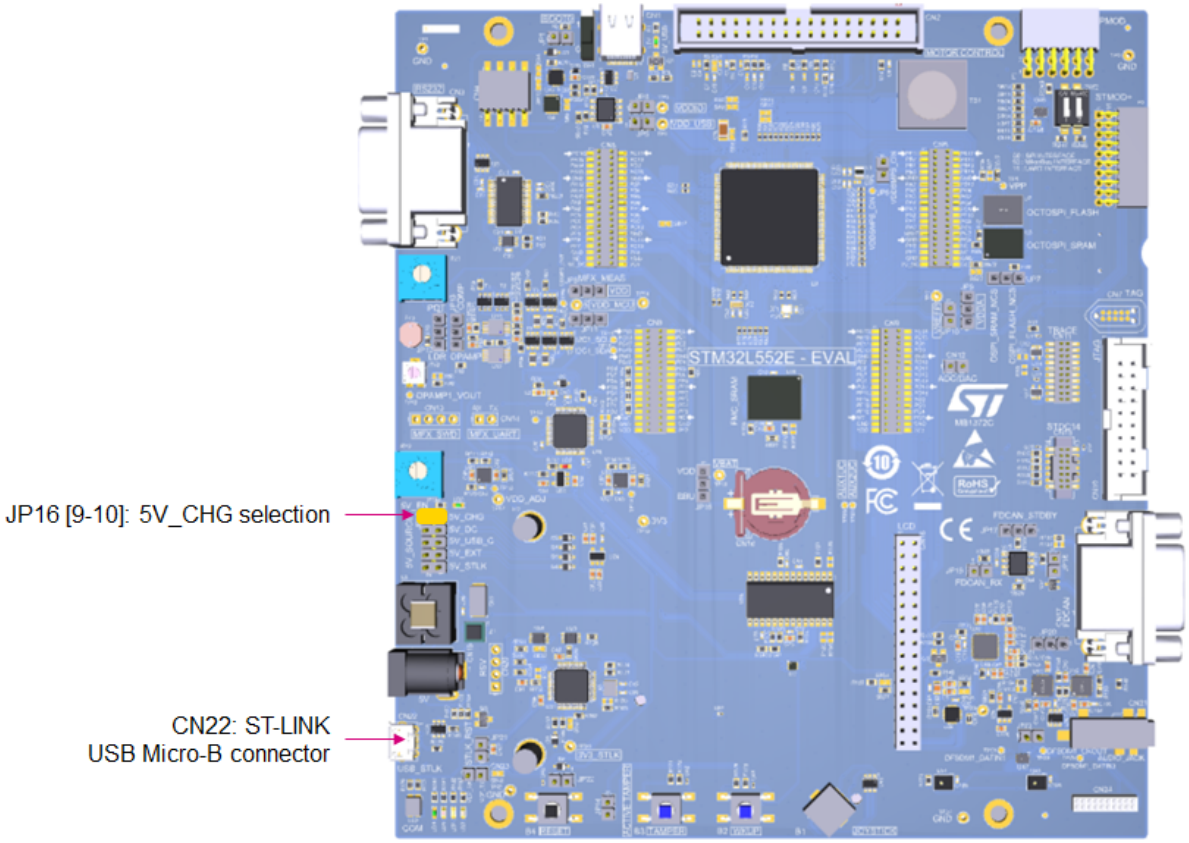


6.6.6 5V_CHG power source

5V_CHG is the DC power charger connected to CN22 USB ST-LINK. To select the 5V_CHG power source on JP16 silkscreen, the jumper of JP16 must be on pins [9-10]. In this case, if the STM32L552E-EV board is powered by an external USB charger, then the debug is not available. If a computer is connected instead of the charger, the current limitation is no more effective. In this case, the computer may be damaged. To avoid this risk, it is recommended to select 5V_STLK mode.

5V_CHG power source configuration for jumper JP16 [9-10] is described in Figure 15.

Figure 15. JP16 [9-10]: CN22 5V_CHG PWR SOURCE



Note: With this JP16 configuration: 5V_CHG, the USB_PWR protection is bypassed. Never used this configuration with a computer connected instead of the charger, because as the USB_PWR_protection is bypassed, and if the board consumption is more than 500mA, this can damage the computer.

Caution: A solder bridge (SB41) can be used to bypass the USB PWR protection switch. (This is not an ST recommended setting). SB41 can be set only when the board is powered by USB PC, and maximum current consumption on 5V_STLINK doesn't exceed 100 mA (including an eventual extension board or ARDUINO® shield). In such a condition, the USB enumeration always succeeds since no more than 100 mA is requested to the PC. Possible SB41 configurations are summarized in Table 13.

Table 13. **USB PWR protection bypass SB41**

SB	Default position[1]	Power supply	Maximum current
SB41	**OFF (not soldered)**	USB PWR through CN22	500 mA limited by Power switch
	ON (soldered)		100 mA maximum
	OFF (not soldered)	5V_EXT or 5V_DC PWR	Whatever the current is. No limitation
	ON (soldered)		Forbidden configuration[2]

1. *The default configuration is shown in bold*
2. *SB41 must be removed when the board is powered by 5V_EXT (CN19) or by 5V_DC (CN5 pin 37 or CN6 pin37).*

Warning:
In case the maximum current consumption of the STM32L552E-EV board with its extension boards exceeds 500 mA, it is recommended to power the STM32L552E-EV board using an external power supply connected to 5V_EXT or 5V_DC.

6.6.7 Programing/debugging when the power supply is not from ST-LINK (5V_STLK)

5V_EXT, 5V_DC or 5V_USB_C can be used as an external power supply in case the current consumption of the STM32L552E-EV with expansion boards exceeds the allowed current on USB. In such a condition, it is still possible to use USB for communication for programming or debugging only.

In this case, it is mandatory to power the board first using 5V_EXT, 5V_DC or 5V_USB_C then connect the USB cable to the PC. Proceeding this way, the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect JP16 jumper according to the external 5V power source selected.
2. Be sure that SB41 is removed.
3. Connect the external power source according to JP16.
4. Power ON the external power supply.
5. Check 5V GREEN LED LD8 is turned ON
6. Connect the PC to the CN22 USB connector

If this sequence is not respected, the board may be powered by V_{BUS} first from ST-LINK, and the following risk may be encountered:

- If more than 500 mA current is needed by the board, the PC may be damaged or current can be limited by PC, As a consequence the board is not powered correctly.
- 500mA is requested at enumeration (since SB41 must be OFF) so there is a risk that request is rejected and enumeration does not succeed if PC does not provide such current. Consequently, the board is not powered (LED LD8 remains OFF).

6.6.8 Power supply output

5V: When the STM32L552E-EV board is powered by USB, 5V_EXT or 5V_DC, the 5V (CN6 pin 38) can be used as an output power supply for an extension board plugged on CN6. In this case, the maximum current of the power source specified in Table 12. Power supply capabilities must be respected.

3V3: CN5 pin 38, CN8 pin 38 or CN9 pin 38 can also be used as power supply output. The current is limited by the maximum current capability of the regulator U23 (ST1L05BPUR from STMicroelectronics) 1,3 A max. concerning the STM32L552E-EV board and its shield consumptions.

6.6.9 Internal Power supply

For all general information concerning Design recommendations for STM32L5 with INTERNAL SMPS, and design guide for ultra-low-power applications with performance, refer to Getting started with *STM32L5 Series hardware developmentL5 Hardware* (AN5211) at the *www.st.com* website.

3V3

Regardless of the 5V power source, an LDO U23 is used to deliver a fixed 3.3 V power supply, with a current capability of 1.3 A. This power source of 3.3 V is shared between the STM32L552E-EV and its expansion boards.

VDD_ADJ

Regardless of the 5 V power source, an LDO U21 is used to deliver an adjust power voltage, with a range of 1.7 to 3.6 V, and a current capability of 1.3 A. This voltage is tuned, thanks to the RV3 potentiometer. This adjustable voltage must be reserved for MCU debugging capability. Be careful to set and select the feature compatible with this adjustable voltage range before updating the board accordingly.

1V8

Regardless of the 5V power source, an LDO U35 is used to deliver a fix 1.8 V voltage, with a current capability of 150 mA. This voltage source is mainly reserved for the low-power audio codec. This one is not targeted to supply the MCU. To drive the MCU in low voltage, use the VDD_ADJ supply voltage.

Caution: The power sequence is not respected when using 1.8 V VDD, refer to the application note AN4555 and the STM32L5xx product datasheets for power sequencing.

Table 14 details the LDO and associated HW SB configuration.

Table 14. LDO and associated HW SB configuration

Solder bridge	Definition	Default position(1)	Comment
SB27	LDO output for 3V3	**ON**	**U23 able to provide the main 3V3**
		OFF	U23 disconnected, no internal 3V3 source
SB26	LDO output for VDD_ADJ	**ON**	**U21 able to provide the main VDD_ADJ: 1V7 to 3V6**
		OFF	U23 disconnected, no internal VDD-ADJ source
SB39	1V8	**ON**	**U35 able to provide audio 1V8**
		OFF	U35 disconnected, no internal audio 1V8 source

1. *The default configuration is shown in bold.*

Table 15 details the MCU power supply configuration and the associated HW configuration.

Table 15. HW configuration for the MCU power supply voltage

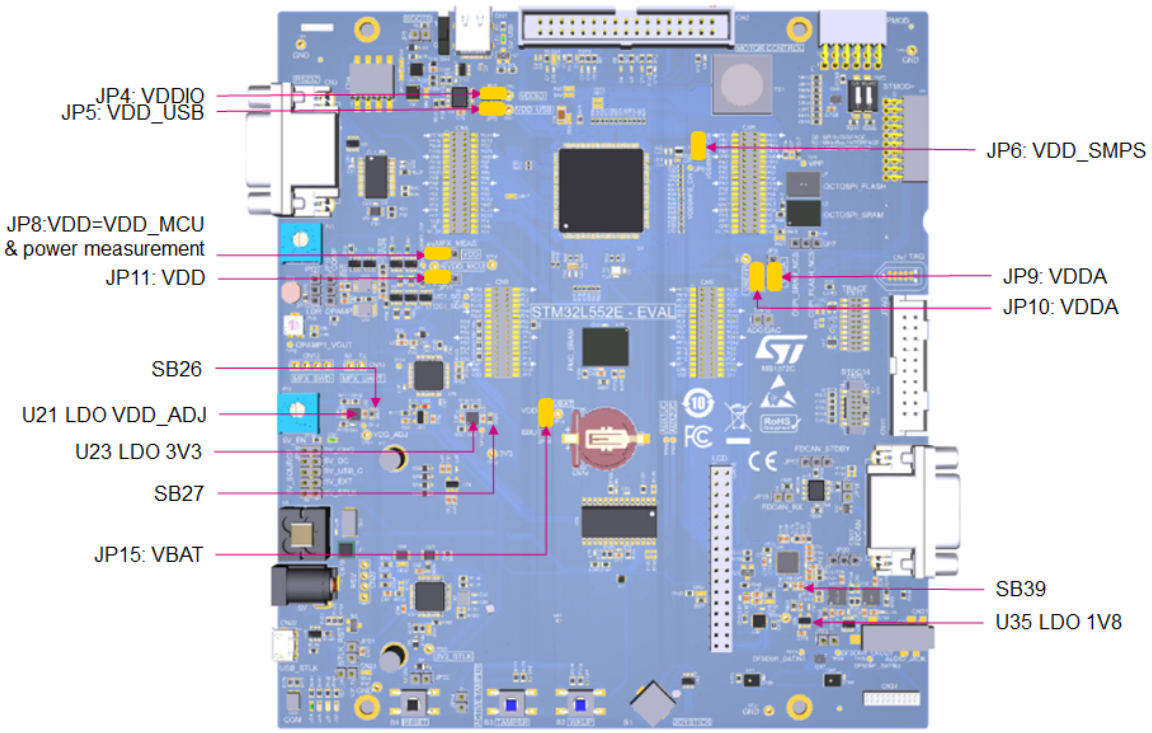
Jumper	Definition	Default position(1)	Comment
JP11	VDD source selection Range 1.7 V < VDD < 3.6 V	**JP11 [1-2]**	**VDD source is fixed at 3.3 V.**
		JP11 [2-3]	VDD source is VDD_ADJ (1.7 V to 3.6 V).
JP8	VDD_MCU power measurement selection Range 1.7 V < VDD_MCU < 3.6 V	**JP8 [1-2]**	**VDD_MCU power measurement selected**
		JP8 [2-3]	VDD_MCU directly connected to VDD, power measurement is bypassed.
JP4	VDDIO source selection for PG [2-15] Range 1.7 V < VDDIO < 3.6 V	**JP4 [1-2]**	**VDDIO source is VDD_MCU.**
		JP4 OFF	VDDIO not supplied or open for debugging or current measurement
JP15	VBAT source selection	**JP15 [1-2]**	**VBAT source is VDD.**

Jumper	Definition	Default position(1)	Comment
JP15	Range 1.7 V < VBAT < 3.6 V	JP15 [2-3]	VBAT source is the external battery.
JP9	VDDA source selection Range 1.7 V < VDDA < 3.6 V	**JP9 [1-2]**	**VDDA source is VDD_MCU.**
		JP9 [2-3]	VDDA source is fixed at 3.3 V.
JP10	VREFP source selection Range 1.7 V < VREFP < 3.6 V	**JP10 [1-2]**	**VREFP source is VDDA.**
		JP10 OFF	VREFP not supplied or open for debugging or current measurement
JP5	VDD_USB source selection Range 3.0 V < VDD_USB < 3.6 V	**JP5 [1-2]**	**VDD_USB source is 3.3 V.**
		JP5 OFF	USB feature not supplied or open for debugging or current measurement
JP6	VDD_SMPS source selection Range 1.7 V < VDDSMPS < 3.6 V	**JP6 [1-2]**	**VDD_SMPS source is VDD_MCU.**
		JP6 OFF	VDD_SMPS not supplied or open for debugging or current measurement.

1. *The default configuration is shown in bold.*

Figure 16 describes the MCU power supplied position on the STM32L552E-EV board.

Figure 16. Jumper and SB for power sources



6.7 Clock references

Two clock references are available on STM32L552E-EV for the STM32L552ZET6QU target microcontroller.

- 32.768 kHz crystal X2, for embedded RTC
- 16 MHz Crystal X1, for HSE clock generator. This one is optional.

The main clock can also be generated using an internal RC oscillator.

Table 16 describes the HW configuration for the 32.768 KHz.

Table 16. HW configuration for the 32.768 KHz

I/O	Solder bridge	Setting[1]	Configuration
PC14	SB110	**Open**	**X2 is used as a clock reference with connected R62.** **PC14 OSC32_IN terminal is not routed to the CN5 extension connector.**
		Closed	PC14 OSC32_IN is routed to the CN5 extension connector. R62 must be removed from X2 quartz circuit to not disturb clock reference or clock source from the daughterboard.
PC15	SB109	**Open**	**X2 is used as a clock reference with connected R63.** **PC15 OSC32_OUT terminal is not routed to the CN5 extension connector.**
		Closed	PC15 OSC32_OUT is routed to the CN5 extension connector. R63 must be removed from the X2 quartz circuit to not disturb clock reference or clock source from the daughterboard.

1. *The default configuration is shown in bold.*

Table 17 describes the HW configuration for the 16 MHz.

Table 17. HW configuration for the 16 MHz

I/O	Solder bridge	Setting[1]	Configuration
PH0	SB120	**Open**	**PH0 OSC_IN terminal is not routed to the CN6 extension connector. X1 can be used as a clock reference.** **SB121 must be open.**
		Closed	PH0 OSC_IN is routed to the CN6 extension connector. R64 and SB121 must be removed, in order not to disturb clock reference or source on the daughterboard.
	SB121	**Open**	**PH0 OSC_IN terminal is not connected to STLINK MCO clock reference.**
		Closed	PH0 OSC_IN is connected to STLINK MCO clock reference. R64 and SB120 must be removed, in order not to disturb MCO clock reference.
PH1	SB119	**Open**	**PH1 OSC_OUT terminal is not routed to the CN6 extension connector. X1 can be used as a clock reference.**
		Closed	PH1 OSC_OUT is routed to the CN6 extension connector. R65 must be removed, in order not to disturb clock reference or source on the daughterboard.

1. *The default configuration is shown in bold.*

6.8 Reset source

The reset signal of the STM32L552E-EV Evaluation board is active low.

Sources of reset are:

- B4 RESET button (black button)
- CN10 JTAG/SWD connector, CN11 TRACE connector, CN15 STDC14 connector, and CN7 TAG connector (reset from debug tools)
- Through CN6 extension connector pin 27 (reset from daughterboard)
- Embedded ST-LINK/V2-1
- Optional (JP22 not fitted) External RS232 interface.

6.9 RSS/bootloader

The bootloader is located in the system memory, programmed by ST during production. It is used to reprogram the Flash memory by using USART, I^2C, SPI, CAN FD or USB FS in device mode through the DFU (device firmware upgrade). The bootloader is available on all devices. Refer to the STM32 microcontroller system memory boot mode application note AN2606 for more details.

The Root Secure Services (RSS) are embedded in a flash area named Secure information block, programmed during ST production. For example, it enables Secure Firmware Installation (SFI) thanks to the RSS extension firmware (RSSe SFI). This feature allows customers to protect the confidentiality of the FW to be provisioned into the STM32 when production is sub-contracted to an untrusted third party. The RSS is available on all devices, after enabling the TrustZone through TZEN option bit.

The bootloader version can be identified by reading the bootloader ID at the address `0x0BF97FFE`.

6.9.1 RSS limitation

The STM32L5 part soldered on STM32L552E-EV with the Finish Good (FG) VAL552E$AU1 (sticker available on the top side of the board) embeds bootloader V9.0 affected by the limitations to be worked around, as described hereunder. The bootloader ID of the bootloader V9.0 is `0x90`.

The following limitations exist in the bootloader V9.0:

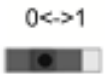
- Option Byte programming in RDP level 0.5 Issue: The user cannot program non-secure option bytes in RDP level 0.5 through the bootloader. Workaround: The user can program option bytes thanks to STM32CubeProgrammer GUI or command-line interfaces through JTAG. To know how to program option bytes through STM32CubeProgrammer, refer to STM32CubeProgrammer user manual UM2237.
- Impossible to set TZEN option bit Issue: The user cannot set the TZEN option bit through Bootloader interfaces. Workaround: Instead of the bootloader interface, the user can use JTAG to set the TZEN option bit.
- Go command on USB-DFU interface Issue: The user cannot use Go command through bootloader on the USB-DFU interface. Workaround: Instead of the USB-DFU interface, the user can use JTAG or any other communication ports supported by Bootloader to run Go command, like USART, I^2C, SPI or CAN FD.

6.9.2 Boot from RSS

The BOOT0 value may come from the PH3_BOOT0 pin, connected to the BOOT switch SW1, or from an option bit depending on the value of a user option bit.

describes the HW configuration for the BOOT mode.

Table 18. Boot selection switch

I/O	Switch	Setting	Description
PH3	SW1		**BOOT0 line is tied low. STM32L552ZET6QU boot address defined by user option bytes NSBOOTADD0 or SECBOOTADD0 according to TrustZone® setting.**
			BOOT0 line is tied high. STM32L552ZET6QU boot address defined by user option bytes NSBOOTADD1 or RSS according to TrustZone® setting.

1. *The default configuration is shown in bold.*

BOOT0 line can also be driven by external equipment connected to the RS-232 connector (pin 6). In this case, the jumper JP1 must be FITTED.

6.10 Audio

A codec CS42L51-CNZ is connected to the SAI interface of STM32L552ZET6QU which supports the TDM feature of the SAI port. The TDM feature offers STM32L552ZET6QU the capability to stream stereo audio channels.

There are two digital microphones on STM32L552E-EV, and the STM32L552E-EV offers the possibility to connect a MEMS extension module.

6.10.1 Operating voltage

The microphones are supplied by VDD and are compatible with the VDD_MCU voltage range from 1.71 to 3.6 V. The audio codec has two supplies:

- VDD_CODEC connected to VDD compatible with VDD_MCU low voltage 1.71 V but limited to a maximum of 3.47 V according to audio codec datasheet
- 1V8_CODEC dedicated 1.8 V source provided by U35

6.10.2 Audio codec interface

The audio codec interface is the MCU SAI1 and also the I2C1 interface.

Table 19 describes the HW configuration for the audio codec interface SAI and I^2C.

Table 19. HW configuration for the audio codec interface SAI and I^2C

I/O	HW	Setting[1]	Configuration
PF6	R219	**ON**	**PF6 is used as SAI1_SD_B to interface the audio codec** No other muxing
PF7	R216	**ON**	**PF7 is used as SAI1_MCLK_B to interface the audio codec.** No other muxing
PF8	R217	**ON**	**PF8 is used as SAI1_SCK_B to interface the audio codec.** No other muxing
PF9	SB98	**ON**	**PF9 is used as SAI1_FS_B to interface the audio codec.**
		OFF	PF9 is not used for the audio codec. PF9 can be used for motor control.
PA10	R202	**ON**	**PA10 is used as SAI1_SD_A to interface the audio codec.** No other muxing
PG13	R232	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**

1. *The default configuration is shown in bold.*

6.10.3 Digital microphones

U39 and U40 on STM32L552E-EV board are IMP34DT05TR MEMS digital omnidirectional microphones providing PDM (pulse density modulation) outputs. To share the same data line, their outputs are interlaced. The combined data output of the microphones is routed to STM32L552ZET6QU terminals, thanks to the integrated input digital filters. The microphones are supplied with the programmable clock directly generated by STM32L552ZET6QU.

The STM32L552ZET6QU DFSDM interface is shared and exclusive between the embedded microphones U39 and U40, the extension module on CN24 connector, the P2 STMOD+ connector and with the two U32 and U33 STPMS2 smart sensors.

Table 20 describes the HW configuration for the DFSDM interface.

Table 20. HW configuration for the DFSDM interface

I/O	HW	Setting[1]	Configuration
-	JP23	**OFF**	**The switch U47 connects directly the DFSDM interface to the onboard MEMS U39 and U40. It is recommended not to have STMOD+ module connected to the P2 connector.**
		ON	DFSDM interface PF10/PD6 is not connected to onboard MEMS. DFSDM is available for the external MEMS module. DFSDM is also connected to STMOD+ or Smart Sensor STPMS2 U32 and U33.
-	MB1299 CN24	**NO external module**	**The switch U47 connects directly the DFSDM interface to the onboard MEMS U39 and U40 (signal DETECTn low, JP23 OFF).**
		External module plug on CN24	The switch U47 disconnect DFSDM to the onboard MEMS U39 and U40, and connect it to the CN24 connector (signal DETECTn switch HIGH by the module). DFSDM is also connected to STMOD+ or smart sensor STPMS2 U32 and U33.
-	P2	**NO external module**	**The switch U47 and JP23 OFF connect directly the DFSDM interface to the onboard MEMS U39 and U40 (signal DETECTn low).**
		External module plug on P2	DFSDM can be used on P2 module, In this configuration, it is recommended to fit the JP23, and not used the CN24 connector. DFSDM can be used on the P2 module.
PD6	R155	ON	DFSDM1_DATIN1 connected to U32 STPMS2L for power metering. In this configuration, it is recommended to fit the JP23, and not used the CN24 connector.
		OFF	**DFSDM1_DATIN1 NOT connected to U32 STPMS2L for power metering.**
PF10	R154	**ON**	**DFSDM1_CKOUT connected to U32 STPMS2L for power metering and U33 STPMS2L for Sigma Delta measurement**
		OFF	DFSDM1_CKOUT NOT connected to U32 STPMS2L for power metering and U33 STPMS2L for Sigma Delta measurement
PC7	R157	**ON**	**DFSDM1_DATIN3 connected to U33 STPMS2L for Sigma Delta measurement**
		OFF	DFSDM1_DATIN3 NOT connected to U33 STPMS2L for Sigma Delta measurement

1. *The default configuration is shown in bold.*

6.10.4 Headphones outputs

The STM32L552E-EV Evaluation board can drive stereo headphones. The STM32L552ZET6QU sends up the stereo audio channels, via its SAI1 TDM port, to the codec device. The codec device converts the digital audio stream to stereo analog signals. It then boosts them for direct drive of headphones connecting to CN21 3.5 mm stereo jack receptacles on the board.

The audio codec is set by an I²C-bus. The address is a 7-bit address, with an additional bit to read or write (High to read, low to write). The AD0 pin connected to GND gives the least significant bit of the address. The address of the audio codec is 0b1001010x. The hexadecimal code is 0x94 to write, and 0x95 to read.

6.10.5 Audio jack connector

Figure 17 shows the CN21 audio jack connector.

Figure 17. CN21 audio jack connector

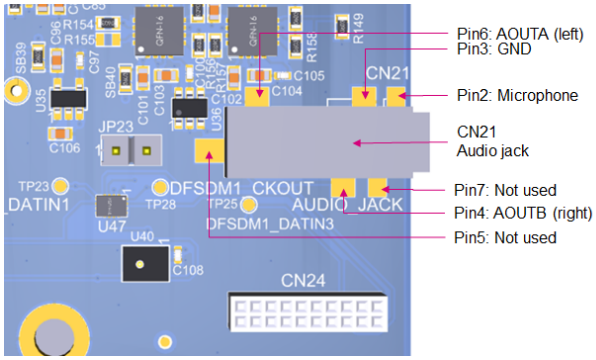


Table 21 describes the CN21 audio jack connector pinout.

Table 21. CN21 audio jack connector pinout

Pin	Board function	Audio codec pin
2	MIC_IN	MICIN1
3	GND	GND
4	AOUTB	AOUTB (RIGHT)
5	NA	NA
6	AOUTA	AOUTA (LEFT)
7	NA	NA

6.10.6 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the AUDIO features:

The AUDIO CODEC cannot be operated simultaneously with motor control.

The MEMS DFSDM cannot be operated simultaneously with DFSDM of the CN24 EXT MEMS module.

The MEMS DFSDM cannot be operated simultaneously with DFSDM of STMOD+.

The MEMS DFSDM cannot be operated simultaneously with DFSDM of STMPS2 U32, U33.

6.11 USB Type-C™ FS port

The STM32L552E-EV Evaluation board supports USB full-speed (FS) communication. The CN1 USB connector is a USB Type-C™ connector.

The STM32L552E-EV Evaluation board supports USB Type-C™ sink mode only.

A green LED LD1 lits up when V_{BUS} is powered by a USB host when the STM32L552E-EV Evaluation board works as a USB device.

6.11.1 Operating voltage

The STM32L552E-EV Evaluation board supports 5 V USB voltage, from 4.75 V to 5.25 V.

MCU VDD_USB only supports the 3.3 V voltage.

6.11.2 USB FS device

When a *USB host* connection to the CN1 USB Type-C™ connector of STM32L552E-EV is detected, the STM32L552E-EV Evaluation board starts behaving as a *USB device*. Depending on the powering capability of the *USB host*, the board can take power from the V_{BUS} terminal of CN1. In the board schematic diagrams, the corresponding power voltage line is called 5V_USB_C.

Section 6.6 Power supply provides information on how to use the powering option.

Table 22 describes the HW configuration for the USB interface.

Table 22. HW configuration for the USB interface

I/O	HW	Setting(1)	Configuration
PA11	R201	**ON**	**PA11 used as USB_FS_N diff pair interface** No other muxing
PA12	R199	**ON**	**PA12 used as USB_FS_P diff pair interface** No other muxing

1. *The default configuration is shown in bold.*

6.11.3 UCPD

USB Type-C™ introduces the USB Power Delivery feature. STM32L552E-EV Evaluation board supports the dead battery and the SINK mode.

In addition to the DP/DM I/Os directly connected to the USB Type-C™ connector, 5 I/Os are also used for UCPD configuration: Configuration Channel (CCx), VBUS-SENSE, UCPD Dead Battery (DBn) and UCPD_FAULT (FLT) feature.

To protect STM32L552E-EV from USB over-voltage, a USB Type-C™ PPS-compliant port protection is used, TCPP01-M12, IC compliant with IEC6100-4-2 level 4.

- Configuration Channel I/O: UCPD_CCx: These signals are connected to the associated CCx line of the USB Type-C™ connector through the STM USB port Protection TCPP01-M12. These lines are used for the configuration channel lines (CCx) to select the USB Type-C™ current mode. STM32L552E-EV only supports SINK current mode.
- Dead Battery I/O: UCPD_DBn: This signal is connected to the associated DBn line of the TCPP01-M12. The STM USB port Protection TCPP01-M12 managed internally the Dead Battery resistors.
- V_{BUS} fault detection: UCPD_FLT: This signal is provided by the STM USB port Protection TCPP01-M12. It is used as fault reporting to MCU after a bad V_{BUS} level detection. By design, the STM32L552E-EV V_{BUS} protection is set to 6 V max.

Table 23 describes the HW configuration for the UCPD interface.

Table 23. HW configuration for the UCPD feature

I/O	HW	Setting(1)	Configuration
PA15	SB73	**ON**	**PA15 connected to USB Type-C™ port protection and used as UCPD_CC1**
		OFF	PA15 NOT used for USB. PA15 can be used for JTAG JTDI.
PB15	R196	**ON**	**PB15 connected to USB Type-C™ port protection and used as UCPD_CC2** No other muxing
PA4	SB107	**ON**	**PA4 used as VBUS_SENSE**
		OFF	PA4 NOT used for USB. PA4 can be used for STMOD+, ADC/DAC or motor control.

I/O	HW	Setting[1]	Configuration
PB5	SB101	**ON**	**UCPD_DBn I/O connected to USB Type-C™ port protection and used as a dead battery feature.**
		OFF	PB5 not used for USB PB5 can be used for COMP or STMOD+.
PB14	R179	**ON**	**UCPD_FLT I/O connected to USB Type-C™ port protection and used as over-voltage fault reporting to MCU** No other muxing

1. *The default configuration is shown in bold.*

6.11.4 USB Type-C™ connector

Figure 18 shows the pinout of the CN1 USB Type-C™ connector.

Figure 18. CN1 USB Type-C™ connector pinout

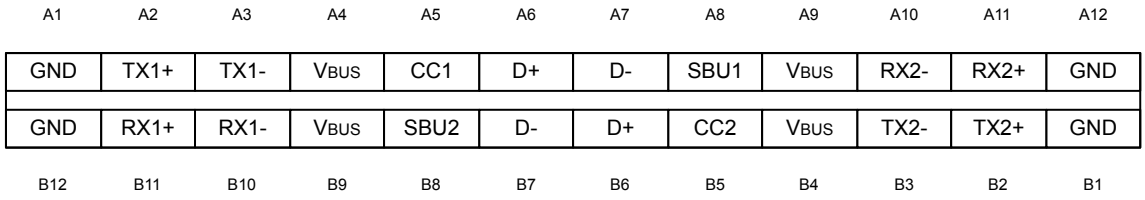


Table 24 describes the pinout of the CN1 USB Type-C™ connector.

Table 24. CN1 USB Type-C™ connector pinout

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
-	GND	A1	B12	GND	-
-	TX1+	A2	B11	RX1+	-
-	TX1-	A3	B10	RX1-	-
-	VBUSc	A4	B9	VBUSc	-
PA15	CC1	A5	B8	SBU2	-
PA12	D+	A6	B7	D-	PA11
PA11	D-	A7	B6	D+	PA12
-	SBU1	A8	B5	CC2	PB15
-	VBUSc	A9	B4	VBUSc	-
-	RX2-	A10	B3	TX2-	-
-	RX2+	A11	B2	TX2+	-
-	GND	A12	B1	GND	-

6.11.5 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the USB features:

The USB UCPD cannot be operated simultaneously with full JTAG (JTDI).

- If PA15 is used as USB_CC1 (USB peripheral), JTDI cannot be used for JTAG peripheral.

The USB UCPD cannot be operated simultaneously with COMPARATOR.

The USB UCPD imposes some restrictions on the STMOD+.

- If PB5 is used as USB_DBn (USB peripheral), COMP2_OUT cannot be used for the COMPARATOR feature, and SPI3_MOSI2 cannot be used for STMOD+ feature.

6.12 RS-232 port

The STM32L552E-EV Evaluation board offers one RS-232 communication port. The RS-232 communication port uses the CN3 DB9 male connector.

6.12.1 Operating voltage

The RS-232 transceiver U6 is supplied by the fix 3V3 power voltage. To support MCU 1V8 I/O configuration, a level shifter U9 is used for the MCU output I/O to reach the transceiver Voltage Input high level (VIH).

In this configuration, the RS-232 interface is fully compatible with the MCU voltage range from 1.71 V to 3.6 V.

6.12.2 RS-232 interface

The RS-232 interface can be connected to either:

- MCU USART3 in 2 wires mode RX, TX
- MCU LPUART1 in 4 wires mode RX, TX, RTS, CTS

Table 25 describes the HW configuration for the RS-232 interface.

Table 25. HW configuration for the RS-232 interface

I/O	HW	Setting[1]	Configuration
PG7	SB49	**ON**	PG7 LPUART1_TX is connected to the RS-232 transceiver. SB50 and SB71 must be not fitted.
		OFF	PG7 LPUART1_TX is NOT connected to the RS-232 transceiver. PG7 can be used for STLINK_VCP.
PG8	SB51	**ON**	**PG8 LPUART1_RX is connected to the RS-232 transceiver.** **SB50 and SB71 must be not fitted.**
		OFF	PG8 LPUART1_RX is not connected to the RS-232 transceiver. PG8 can be used for STLINK_VCP.
PB10	SB77	ON	PB10 USART3_TX is connected to the RS-232 transceiver. SB49 and SB78 must be not fitted.
		OFF	**PB10 USART3_TX is NOT connected to the RS-232 transceiver.** **PB10 can be used for STLINK_VCP.**
PB11	SB71	ON	PB11 USART3_RX is connected to the RS-232 transceiver. SB51 and SB75 must be not fitted.
		OFF	**PB11 USART3_RX is NOT connected to the RS-232 transceiver.** **PB11 can be used for STLINK_VCP.**
PB13	R190 / R44	**ON**	**PB13: LPUART1_CTS is connected to the RS-232 transceiver and STMOD+.**
PG6	R203	**ON**	**PG6: LPUART1_RTS is connected to the RS-232 transceiver and STMOD +.**

1. *The default configuration is shown in bold.*

Figure 19 shows the CN3 RS-232 connector pinout.

Figure 19. **CN3 RS-232 connector pinout**

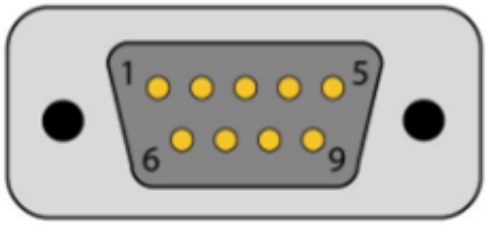


Table 26 describes the CN3 RS-232 connector pinout.

Table 26. **CN3 RS-232 connector pinout**

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
NC	NC	1	6	BOOTLOADER_BOOT0	PH3_BOOT0
PG8 / PB11	LPUART_RX or USART_RX	2	7	LPUART1_RTS	PG6
PG7 / PB10	LPUART_TX or USART_TX	3	8	LPUART1_CTS	PB13
NC	NC	4	9	NC	NC
GND	GND	5	-	-	-

6.12.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the RS-232 features:

It is not recommended to put the RS-232 AND the STLINK-VCP on the same UART: One must be on LPUART and the other one on the USART3,: and vice versa.

The RS-232 cannot be operated simultaneously with the STMOD+_UART.

6.13 microSD™ card

The CN25 slot for the microSD™ card is routed to the STM32L552ZET6QU SDIO port. This interface is compliant with SD Memory Card Specification Version 4.1: SDR104 SDMMC_CK speed limited to the maximum allowed I/O speed. UHS-II mode is not supported. The microSD™ card interface is on the bottom side of the board.

6.13.1 Operating voltage

The SD card interface is only compatible with the 3.3 V voltage range, from 2.7 to 3.6 V.

The SD card interface does not support the MCU low voltage 1.8 V range.

6.13.2 SD card interface

The SD card interface is used in 4 data lines D [0:3], one CLK, one CDM, and a card detection signal.

Table 27 describes the HW configuration for the SDIO interface.

Table 27. HW configuration for the SDIO interface

I/O	HW	Setting[1]	Configuration
PG10	SB61	**ON**	**PG10 is connected to SDCARD DETECT.**
		OFF	PG10 is not connected to SDCARD DETECT. PG10 can be used for STMOD+.
PC8	SB56	**ON**	**PC8 is connected to SDCARD SDIO1_D0.**
		OFF	PC8 is not connected to SDCARD SDIO1_D0. PC8 can be used for motor control.
PC9	SB58	**ON**	**PC9 is connected to SDCARD SDIO1_D1.**
		OFF	PC9 is not connected to SDCARD SDIO1_D1. PC9 can be used for TRACE.
PC10	SB67	**ON**	**PC10 is connected to SDCARD SDIO1_D2.**
		OFF	PC10 is not connected to SDCARD SDIO1_D2. PC10 can be used for TRACE.
PC12	SB63	**ON**	**PC12 is connected to SDCARD SDIO1_CLK.**
		OFF	PC12 is not connected to SDCARD SDIO1_CLK. PC12 can be used for TRACE or STMOD+.
PC11	R187	**ON**	**PC11 is connected to SDCARD SDIO1_D3.** No other muxing
PD2	R188	**ON**	**PD2 is connected to SDCARD SDIO1_CMD.** No other muxing

1. *The default configuration is shown in bold.*

Figure 20 shows the CN25 SD card connector pinout.

Figure 20. CN25 SD card connector pinout

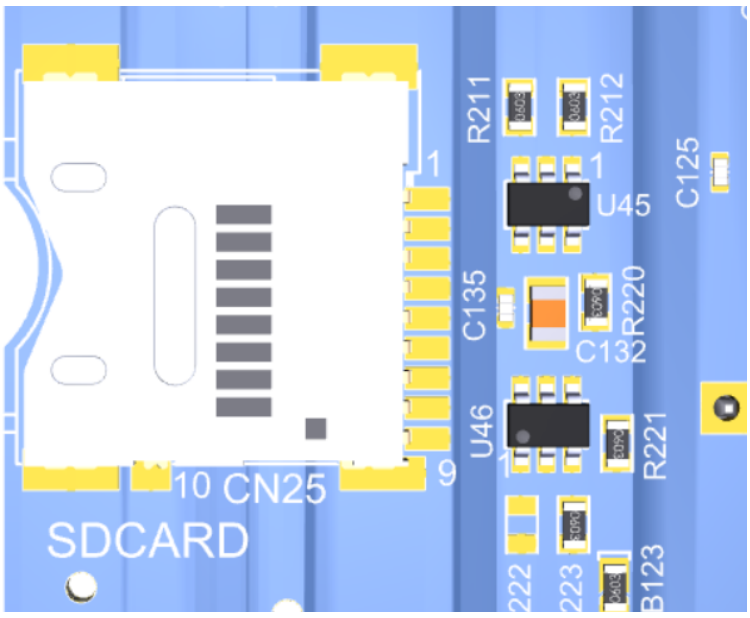


Table 28 describes the CN25 SD card connector pinout.

Table 28. CN25 SD card connector pinout

Pin	Board function	STM32 pin
1	SDIO1_D2	PC10
2	SDOI1_D3	PC11
3	SDIO1_CMD	PD2
4	VDD_SDCARD	-
5	SDIO1_CLK	PC12
6	GND	-
7	SDIO1_D0	PC8
8	SDIO1_D1	PC9
9	GND for DETECT pin	-
10	SDCARD_DETECT active LOW	PG10

6.13.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the SDIO features:

The microSD™ card cannot be operated simultaneously with the motor-control function.

The microSD™ card cannot be operated simultaneously with the TRACE function.

The microSD™ card cannot be operated simultaneously with the STMOD+ (SPI) function.

6.14 CAN FD

The STM32L552E-EV Evaluation board supports one CAN FD compliant with ISO-11898-1 version 2.0 parts A and B. The CN17 DB9 male connector is available as a CAN-FD interface.

6.14.1 Operating voltage

A 3.3 V CAN transceiver is fitted between the CN17 connector and the CAN-FD controller port of STM32L552ZET6QU.

In this configuration, the CAN-FD interface is compatible with the MCU voltage range, from 1.8 V to 3.6 V (Low voltage 1.71 V does not fit with the CAN transceiver specification).

6.14.2 CAN-FD interface

The JP17 jumper allows selecting one of high-speed, standby and slope control modes of the CAN transceiver. The JP18 jumper can fit a CAN termination resistor (R125). The JP19 is used to connect CAN transceiver avoiding unknown signals from CAN-FD transceiver.

Table 29 describes the HW configuration for the CAN FD.

Table 29. HW configuration between MCU and CAN-FD transceiver

I/O	HW	Setting[1]	Configuration
-	JP17	**JP17 [1-2]**	**CAN transceiver operates in high-speed mode**
		JP17 [2-3]	CAN transceiver is in standby mode
-	JP18	**ON**	**Termination resistor fitted on CAN physical link**
		OFF	No termination resistor on CAN physical link
PB8	JP19	**ON**	**PB8: FDCAN_RX is used from STM32L552ZET6QU terminal**
		OFF	PB8 is not used for CAN transceiver. No other muxing
PB9	R210	**ON**	**PB9: FDCAN_TX is used as FDCAN_TX.**
	-	OFF	PB9 is not used for CAN transceiver. No other muxing

1. *The default configuration is shown in bold.*

Figure 21 shows the CN17 CAN-FD connector pinout.

Figure 21. CN17 CAN-FD connector pinout

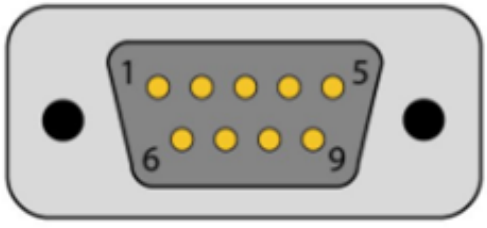


Table 30 describes the CN17 CAN-FD connector pinout.

Table 30. CN17 CAN-FD interface and connector pinout

CAN transceiver	Board function	Pin	Pin	Board function	CAN transceiver
-	NC	1	6	GND	-
CANL	CANL	2	7	CANH	CANH
-	GND	3	8	NC	-
-	NC	4	9	NC	-
-	GND	5	-	-	-

6.14.3 I/O restriction to other features

There is no limitation for the CAN-FD interface link to the I/O muxing.

6.15 Smartcard

The STM32L552E-EV Evaluation board supports one smartcard interface. The CN26 smartcard connector is used as a card reader. The smartcard interface is on the bottom side of the board.

6.15.1 Operating voltage

The smartcard interface is only compatible from 2.7 V to 3.6 V MCU range. Low power MCU 1.8 V is not supported by the smartcard interface.

6.15.2 Smartcard interface

A smartcard interface is used between the CN26 card reader connector and the smartcard controller port of STM32L552ZET6QU.

Table 31 describes the HW configuration for the smartcard interface.

Table 31. HW configuration for the smartcard interface

I/O	Solder bridge	Setting[1]	Configuration
PA9	SB65	**ON**	**PA9 is connected to the smartcard interface as SMARTCARD_IO.**
		OFF	PA9 is not connected to the smartcard interface. PA9 can be used for motor control.
PA8	R205	**ON**	**PA8 is connected to the smartcard interface as SMARTCARD_CLK** No other muxing
MFX_IO6	-	-	**MFX_IO6 used as SMARTCARD_OFF** No other muxing
MFX_IO7	-	-	**MFX_IO7 used as SMARTCARD_RST** No other muxing
MFX_IO9	-	-	**MFX_IO9 used as SMARTCARD_CMDVCC** No other muxing
MFX_IO10	-	-	**MFX_IO10 used as SMARTCARD_3/5V** No other muxing

1. *The default configuration is shown in bold.*

Figure 22 shows the CN26 smartcard connector pinout.

Figure 22. U26 smartcard connector pinout

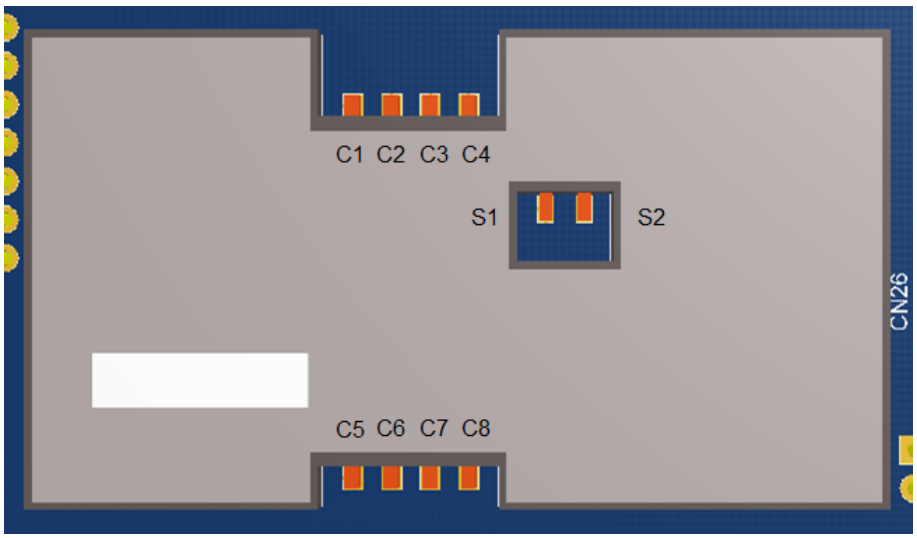


Table 32 describes the U26 smartcard interface and CN26 connector pinout.

Table 32. U26 smartcard interface and CN26 connector pinout

Pin	Board function	U26 smartcard interface pin
C1	VCC: card supply	U26-17
C2	RST: card reset	U26-16
C3	CLK: card clock	U26-15
C4	NC	-
C5	GND: card GND	U26-14
C6	NC	-
C7	I/O card data	U26-11
C8	NC	-
S1	GND: card GND	GND
S2	DETECT: card-detect (LOW)	U26-9

6.15.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the smartcard features:

The smartcard card cannot be operated simultaneously with the motor-control function.

6.16 User LEDs

Four general-purpose color LEDs (LD4, LD5, LD6, LD7) are available as light indicators. Each LED is in light-emitting state when a low level is applied to the corresponding ports.

Two user LEDs, the green LD4 and red LD5 LEDs are directly connected to the STM32L552ZET6QU.

The two other user LEDs yellow LED LD6 and orange LED LD7 are connected to the MFX IO-expander.

6.16.1 Operating voltage

As LEDs are driven by the I/O LOW level, they are compatible with VDD_MCU 1.8 V.

Caution: With this configuration, consumption is not optimized because of the I/Os at 1.8 V and LEDs VDD at 3.3 V. A small leakage current can appear.

6.16.2 LED interface

Table 33 describes the HW configuration for the LED interface.

Table 33. HW configuration for the LED interface

I/O	Solder bridge	Setting[1]	Configuration
PB3	SB82	**ON**	**Active low PB3 is connected to the green LED LD4.**
		OFF	PB3 is not connected to the LED. PB3 can be used for JTAG.
PD3	R102	**ON**	**Active low PD3 is connected to the red LED LD5.** No other muxing
MFX_IO11	-	-	**Active low MFX_IO11 is connected to the yellow LED LD6.** No other muxing
MFX_IO13	-	-	**Active low MFX_IO13 is connected to the orange LED LD7.** No other muxing

1. *The default configuration is shown in bold.*

6.16.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the LED features:

The green LED I/O cannot be operated simultaneously with JTAG SWO.

6.17 Physical input devices: buttons

The STM32L552E-EV Evaluation board provides a number of input devices for physical human control. These are:

- A four-way joystick controller with select key (B1)
- A wake-up button (B2)
- A tamper button (B3)
- A Reset button (B4)

6.17.1 Operating voltage

Input devices for physical human control are connected to VDD or are referenced to GND. So input devices are compatible with VDD_MCU voltage range from 1.71 V to 3.6 V.

6.17.2 Physical input I/O interface

Table 34 describes the HW configuration for the physical user interface.

Table 34. HW configuration for the physical user interface

I/O	HW	Setting[1]	Configuration
PA1	SB114	**ON**	**Active high PA1 is connected to the TAMPER KEY button B3 as TAMPER function.**
		OFF	PA1 is not connected to the TAMPER KEY. PA1 can be used for OPAMP, STMOD+ or motor control.
PC13	JP14	**OFF**	**Active high PC13 is connected to Wakeup button B2.**
		ON	Active TAMPER function between PA1 and PC13
NRST	-	-	**Active low button RESET source**

I/O	HW	Setting(1)	Configuration
MFX _IO2	-	-	**JOY_LEFT: Joystick left direction connected to B1 pin1**
MFX_IO0	-	-	**JOY_SEL: Joystick selection connected to B1 pin2**
MFX_IO1	-	-	**JOY_DOWN: Joystick down direction connected to B1 pin3**
MFX_IO4	-	-	**JOY_UP: Joystick up direction connected to B1 pin4**
MFX_IO3	-	-	**JOY_RIGHT: Joystick right direction connected to B1 pin6**

1. *The default configuration is shown in bold.*

6.17.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the physical interface features:

- The TAMPER KEY function cannot be operated simultaneously with the TAMPER LOOP, the OPAMP, the STMOD+ or the motor-control functions.
- The WAKEUP Button function cannot be operated simultaneously with the TAMPER LOOP function.

6.18 Operational amplifier and comparator

The STM32L552E-EV Evaluation board offers the possibility to test internal operational amplifier and comparator according to: :

- a 10 kΩ potentiometer (RV1)
- a light-dependent resistor, LDR (R73)

The potentiometer and the light-dependent resistor can be routed, mutually exclusively, to either PB4 (COMP) or to PA0 (OPAMP) port of STM32L552ZET6QU.

6.18.1 Operating voltage

Input devices for physical human control are connected to VDD or referenced to GND. So input devices are compatible with VDD_MCU range from 1.71 to 3.6 V.

6.18.2 Operational amplifier

STM32L552ZET6QU provides two onboard operational amplifiers. One of which, OpAmp1, is made accessible on STM32L552E-EV. OpAmp1 has its inputs and its output routed to I/O ports.

Table 35 describes the HW configuration for the OPAMP interface

Table 35. HW configuration for the OPAMP interface

I/O	HW	Setting(1)	Configuration
PA0	SB116	**ON**	**PA0 is used as OPAMP1_INP and connected to JP13 pin 3.**
		OFF	PA0 is not used as OPAMP. PA0 can be used for MFX, STMOD+ or motor control.
PA1	SB111	**ON**	**PA1 is used as OPAMP1_INM and connected to adjust resistor bridge R98 / RV2.**
		OFF	PA1 is not used as OPAMP PA1 can be used for TAMPER KEY, STMOD+ or motor control.
PA3	SB84	ON	PA3 is used as OPAMP1_VOUT and connected to TP13.
		OFF	**PA3 is not used as OPAMP** **PA3 can be used for Octo-SPI or motor control.**

1. *The default configuration is shown in bold.*

The non-inverting input PA0 is accessible on the pin 3 of the JP13 jumper header. On top of the possibility of routing, either of the potentiometer or LDR to PA0, an external source can also be connected to it, using the terminal 3 of JP13.

The PA3 output of the operational amplifier can be accessed on test point TP13. Refer to the schematic of the STM32L552E-EV.

The gain of OpAmp1 is determined by the ratio of the variable resistor RV2 and the resistor R98, as shown in the following equation: `Gain = 1+ RV2/R98`

With the RV2 ranging from 0 to 10 kΩ and R98 being 1 kΩ, the gain can vary from 1 to 11.

The R92 resistor in series on PA0 is beneficial for reducing the output offset.

Table 36 describes the jumper configuration to enable the LDR or the potentiometer to OPAMP1 function.

Table 36. Jumper configuration to enable the LDR or the potentiometer to OPAMP1 function

HW	Setting(1)	Configuration
JP12 / JP13	**JP12 [1-2] / JP13 [2-3]**	**Potentiometer RV1 is routed to pin OPAMP1_INP PA0 of STM32L552ZET6QU.**
	JP12 [2-3] / JP13 [2-3]	LDR is routed to pin OPAMP1_INP PA0 of STM32L552ZET6QU.

1. *The default configuration is shown in bold.*

6.18.3 Comparator

STM32L552ZET6QU provides two onboard comparators. One of which, COMP2, is made accessible on STM32L552E-EV. COMP2 has its non-inverting input and its output.

Table 37 describes the HW configuration for the comparator interface

Table 37. HW configuration for the comparator interface

I/O	HW	Setting(1)	Configuration
PB4	SB92	**ON**	**PB4 is used as COMP2_INP and connected to JP13 pin 1.**
		OFF	PB4 is not used as a COMP input. PB4 can be used for JTAG or STMOD.
PB5	SB103	**ON**	**PB5 is used as COMP2_OUT and connected to TP8.**
		OFF	PB5 is not used as a COMP input. PB5 can be used for USB or STMOD+.

1. *The default configuration is shown in bold.*

The input is accessible on the pin 1 of the JP13 jumper header. On top of the possibility of routing either the potentiometer or LDR to PB4, an external source can also be connected to it, using the terminal 1 of JP13.

The PB5 output of the comparator can be accessed on test point TP8. Refer to the schematic of STM32L552E-EV.

Table 38 describes the jumper configuration to enable the LDR or the potentiometer to COMP2 function.

Table 38. Jumper configuration to enable the LDR or the potentiometer to COMP2 function

HW	Setting(1)	Configuration
JP12 / JP13	**JP12 [1-2] / JP13 [1-2]**	**Potentiometer RV1 is routed to pin PB4 of STM32L552ZET6QU.**
	JP12 [2-3] / JP13 [1-2]	LDR is routed to pin PB4 of STM32L552ZET6QU.

1. *The default configuration is shown in bold.*

6.18.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the OPAMP and COMP features:

- OPAMP cannot be operated simultaneously with the TAMPER KEY, MFX, Octo-SPI, STMOD+ or motor-control functions.
- COMP cannot be operated simultaneously with the JTAG STMOD+ and USB UCPD functions.

6.19 Analog input, output, VREF

STM32L552E-EV provides onboard analog-to-digital converter ADC, and digital-to-analog converter DAC. The port PA4 can be configured to operate either as ADC input or as DAC output. PA4 is routed to the CN12 two-way header allowing to fetch signals to or from PA4 or to ground it by fitting a jumper into CN12.

6.19.1 ADC/DAC I/O interface

Parameters of the ADC input low-pass filter formed with R233 and C141 can be modified by replacing these components according to application requirements.

Similarly, parameters of the DAC output low-pass filter formed with R224 and C141 can be modified by replacing these components according to application requirements.

The VREFP terminal of STM32L552ZET6QU is used as the reference voltage for both ADC and DAC. By default, it is routed to VDDA through a jumper fitted into the two-way header JP10. The jumper can be removed and an external voltage applied to the terminal 2 of JP10, for specific purposes.

Table 39 describes the HW configuration for the ADC/DAC interface

Table 39. HW configuration for the ADC/DAC interface

I/O	HW	Setting[1]	Configuration
PA4	SB124	**ON**	**PA4 is used as ADC/DAC and connected to CN12 pin 1.**
		OFF	PA4 is not used as ADC/DAC PA4 can be used for USB, STMOD+, or motor control.
VREFP	JP10	**ON**	**VDDA used as ADC/DAC power supply.**
		OFF	ADC/DAC not powered

1. *The default configuration is shown in bold.*

Table 40 describes the jumper configuration for ADC/DAC interface.

Table 40. CN12 ADC/DAC interface and connector pinout

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
PA4	ADC/DAC	1	2	GND	-

6.19.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the ADC/DAC button features:

- ADC/DAC cannot be operated simultaneously with UCPD function.
- ADC/DAC cannot be operated simultaneously with STMOD+ function.
- ADC/DAC cannot be operated simultaneously with the motor-control function.

6.20 SRAM device

IS61WV102416BLL, a 16-Mbit static RAM (SRAM), 1 M x16 bit, is fitted on the STM32L552E-EV, in the U15 position.

6.20.1 Operating voltage

The SRAM is only functional to the voltage range from 2.4 to 3.6 V, according to the SRAM datasheet.

This SRAM does not support the low voltage MCU 1.8 V.

6.20.2 SRAM interface

STM32L552E-EV and the addressing capabilities of FMC allow hosting SRAM devices up to 32 Mbytes. This is the reason why the schematic of STM32L552E-EV mentions several SRAM devices.

The SRAM device is attached to the 16-bit data bus and accessed with FMC. The base address is `0x6000 0000`, corresponding to NOR/SRAM1 bank1. The SRAM device is selected with the FMC_NE1 chip select. FMC_NBL0 and FMC_NBL1 signals allow selecting 8-bit and 16-bit data word operating modes.

Table 41 describes the HW configuration for the SRAM interface.

Table 41. HW configuration for the SRAM interface

I/O	HW	Setting(1)	Configuration
PD7	R94	**ON**	**PD7 is used as FMC_NE1 and connected to SRAM.**
PD5	R239	**ON**	**PD5 is used as FMC_NWE and connected to SRAM and LCD.**
PD4	R101	**ON**	**PD4 is used as FMC_NOE and connected to SRAM and LCD.**
PE0	R227	**ON**	**PE0 is used as FMC_NBL0 and connected to SRAM.**
PE1	R226	**ON**	**PD4 is used as FMC_NBL1 and connected to SRAM.**
PD14	R23	**ON**	**PD14 is used as FMC_D0 and connected to SRAM and LCD.**
PD15	R22	**ON**	**PD15 is used as FMC_D1 and connected to SRAM and LCD.**
PD0	R33	**ON**	**PD0 is used as FMC_D2 and connected to SRAM and LCD.**
PD1	R35	**ON**	**PD1 is used as FMC_D3 and connected to SRAM and LCD.**
PE7	R48	**ON**	**PE7 is used as FMC_D4 and connected to SRAM and LCD.**
PE8	R46	**ON**	**PE8 is used as FMC_D5 and connected to SRAM and LCD.**
PE9	R45	**ON**	**PE9 is used as FMC_D6 and connected to SRAM and LCD.**
PE10	R43	**ON**	**PE10 is used as FMC_D7 and connected to SRAM and LCD.**
PE11	R41	**ON**	**PE11 is used as FMC_D8 and connected to SRAM and LCD.**
PE12	R40	**ON**	**PE12 is used as FMC_D9 and connected to SRAM and LCD.**
PE13	R38	**ON**	**PE13 is used as FMC_D10 and connected to SRAM and LCD.**
PE14	R36	**ON**	**PE14 is used as FMC_D11 and connected to SRAM and LCD.**
PE15	R34	**ON**	**PE15 is used as FMC_D12 and connected to SRAM and LCD.**
PD8	R29	**ON**	**PD8 is used as FMC_D13 and connected to SRAM and LCD.**
PD9	R28	**ON**	**PD9 is used as FMC_D14 and connected to SRAM and LCD.**
PD10	R27	**ON**	**PD10 is used as FMC_D15 and connected to SRAM and LCD.**
PF0	R77	**ON**	**PF0 is used as FMC_A0 and connected to SRAM.**
PF1	R78	**ON**	**PF1 is used as FMC_A1 and connected to SRAM.**
PF2	R79	**ON**	**PF2 is used as FMC_A2 and connected to SRAM.**
PF3	R80	**ON**	**PF3 is used as FMC_A3 and connected to SRAM.**
PF4	R81	**ON**	**PF4 is used as FMC_A4 and connected to SRAM.**
PF5	R82	**ON**	**PF5 is used as FMC_A5 and connected to SRAM.**
PF12	R57	**ON**	**PF12 is used as FMC_A6 and connected to SRAM.**
PF13	R56	**ON**	**PF13 is used as FMC_A7 and connected to SRAM.**

I/O	HW	Setting[1]	Configuration
PF14	R55	**ON**	**PF14 is used as FMC_A8 and connected to SRAM.**
PF15	R54	**ON**	**PF15 is used as FMC_A9 and connected to SRAM.**
PG0	R52	**ON**	**PG0 is used as FMC_A10 and connected to SRAM.**
PG1	R50	**ON**	**PG1 is used as FMC_A11 and connected to SRAM.**
PG2	R21	**ON**	**PG2 is used as FMC_A12 and connected to SRAM.**
PG3	R32	**ON**	**PG3 is used as FMC_A13 and connected to SRAM.**
PG4	R31	**ON**	**PG4 is used as FMC_A14 and connected to SRAM.**
PG5	R30	**ON**	**PG5 is used as FMC_A15 and connected to SRAM.**
PD11	R26	**ON**	**PD11 is used as FMC_A16 and connected to SRAM.**
PD12	R25	**ON**	**PD12 is used as FMC_A17 and connected to SRAM.**
PD13	R24	**ON**	**PD13 is used as FMC_A18 and connected to SRAM.**
PE3	R66	**ON**	**PE3 is used as FMC_A19 and connected to SRAM.**
PE4	R67	**ON**	**PE4 is used as FMC_A20 and connected to SRAM.**

1. *The default configuration is shown in bold.*

6.20.3 I/O restriction to other features

By default, only an SRAM of 16 Mbits is present on the STM32L552E-EV board. An update of the SRAM (footprint compatible) is possible to increase the memory up to 32MBits A[0-20].

The FMC interface is shared with LCD.

6.21 Octo-SPI memories device

6.21.1 Octo-SPI Flash memory device

MX25LM51245GXDI00, a 512-Mbit Octo-SPI Flash memory device, is fitted on STM32L552E-EV, in the U7 position. It is used when evaluating the STM32L552ZET6QU Octo-SPI interface.

MX25LM51245GXDI00 can operate in both single (STR) and double (DTR) transfer rate modes.

6.21.2 Octo-SPI Flash SRAM device

IS66WVH8M8BLL-100B1LI, a 64-Mbit self-refresh static random access memory (SRAM) device with a HyperBus™ interface, is fitted on STM32L552E-EV, in the U8 position. It is used when evaluating the STM32L552ZET6QU Octal-SPI interface with HyperBus™.

6.21.3 Operating voltage

The voltage of the Octo-SPI Flash memory device MX25LM51245GXDI00 is in the range of 2.7 to 3.6 V.

The voltage of the Octo-SPI SRAM device IS66WVH8M8BLL-100BLI is in the range of 2.7 to 3.6 V.

The OCTO-SPI memory does not support the low voltage MCU 1.8 V.

6.21.4 Octo-SPI I/O interface

Table 42 describes the HW configuration for the Octo-SPI interface.

Table 42. HW configuration for the Octo-SPI interface

I/O	Resistor	Setting[1]	Configuration
PA2	R208	**ON**	**PA2 is connected to Octo-SPI memories as NCS.**
		OFF	PA2 is NOT connected to Octo-SPI memories. PA2 can be used for motor control.
PA3	R206	**ON**	**PA3 is connected to Octo-SPI memories as CLK.**
		OFF	PA3 is NOT connected to Octo-SPI memories. PA3 can be used for OPAMP or motor control.
PA6	R204	**ON**	**PA6 is connected to Octo-SPI memories as IO3.**
		OFF	PA6 is NOT connected to Octo-SPI memories. PA6 can be used for motor control.
PA7	R198	**ON**	**PA7 is connected to Octo-SPI memories as IO2.**
		OFF	PA7 is not connected to Octo-SPI memories. PA7 can be used for motor control.
PB0	R195	**ON**	**PB0 is connected to Octo-SPI memories as IO1**
		OFF	PB0 is NOT connected to Octo-SPI memories. PB0 can be used for motor control.
PB1	R194	**ON**	**PB1 is connected to Octo-SPI memories as IO0.**
		OFF	PB1 is NOT connected to Octo-SPI memories. PB1 can be used for motor control.
PB2	R189	**ON**	**PB2 is connected to Octo-SPI memories as DQS.**
		OFF	PB2 is NOT connected to Octo-SPI memories. PB2 can be used for motor control.
PC0	R209	**ON**	**PC0 is connected to Octo-SPI memories as IO7.**
		OFF	PC0 is NOT connected to Octo-SPI memories. PC0 can be used for motor control.
PC1	R215	**ON**	**PC1 is connected to Octo-SPI memories as IO4.**
		OFF	PC1 is NOT connected to Octo-SPI memories. PC1 can be used for motor control.
PC2	R214	**ON**	**PC2 is connected to Octo-SPI memories as IO5.**
		OFF	PC2 is NOT connected to Octo-SPI memories. PC2 can be used for motor control.
PC3	R218	**ON**	**PC3 is connected to Octo-SPI memories as IO6.**
		OFF	PC3 is NOT connected to Octo-SPI memories. PC3 can be used for motor control.
PF11	SB22	**ON**	**PF11 is connected to Octo-SPI SRAM NCS.** **JP7 must be in [1-2] in this configuration.**
		OFF	PF11 is NOT connected to Octo-SPI SRAM NCS. PF11 can be used for optional Octo-SPI SRAM 1V8 for CLK-N.

I/O	Resistor	Setting[1]	Configuration
PF11	SB23	ON	PF11 is connected to Octo-SPI SRAM CLK-N for 1V8.
		OFF	**PF11 is NOT connected to Octo-SPI SRAM CLK-N for 1V8.**

1. *The default configuration is shown in bold.*

Table 43 describes the jumper configuration to enable the Octo-SPI function.

Table 43. Octo-SPI jumper configuration

HW	Setting[1]	Configuration
JP7	**JP7 [1-2]**	**PA2: OCTOSPI_NCS is connected to the Octo-SPI FLASH CS pin.**
	JP7 [2-3]	PA2: OCTOSPI_NCS is connected to the Octo-SPI SRAM CS pin. In this configuration, SB22 must be removed.

1. *The default configuration is shown in bold.*

6.21.5 I/O restriction to other features

Caution: Due to the share of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the Octo-SPI features:

- The Octo-SPI function cannot be operated simultaneously with the motor-control function.
- The Octo-SPI function cannot be operated simultaneously with OPAMP function.

6.22 EEPROM

M24128-DFMN6TP, a 128-Kbit I²C-bus EEPROM device, is fitted on the main board of STM32L552E-EV, in U3 position. It is accessed with I²C-bus lines I2C1_SCL and I2C1_SDA of STM32L552ZET6QU. It supports all I²C-bus modes with speeds up to 1 MHz. The base I²C-bus address is `0xA0`. Write-protecting the EEPROM is possible through opening the SB13 solder bridge. By default, SB13 is closed and writing into the EEPROM enabled.

6.22.1 Operating voltage

The M24128-DFDW6TP EEPROM device's operating voltage is fully compatible with the MCU voltage range from 1.71 to 3.6 V.

6.22.2 EEPROM I/O interface

Table 44 describes the HW configuration for the EEPROM interface.

Table 44. HW configuration for the EEPROM interface

I/O	Resistor	Setting[1]	Configuration
PG13	R232	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**

1. *The default configuration is shown in bold.*

6.23 EXT_I2C connector

CN4 EXT_I2C connector can be connected to the I²C bus daughterboard. MFX_GPIO8 of MFX MCU provides EXT_RESET.

6.23.1 Operating voltage

CN4 connector pin 4 is connected to VDD. So the external module must be compliant with the VDD range used on the MCU: normal voltage range from 2.7 to 3.3 V, or low voltage range from 1.7 to 3.3 V.

6.23.2 EXT_I2C I/O interface

Table 45 describes the HW configuration for the EXT_I2C interface.

Table 45. HW configuration for the EXT_I2C interface

I/O	Resistor	Setting[1]	Configuration
PG13	R232	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
MFX_IO8	-	**-**	**MFX_IO8 connected to CN4 as EXT_RESET**

1. *The default configuration is shown in bold.*

Figure 23 shows the CN4 EXT_I2C connector pinout.

Figure 23. CN4 EXT_I2C connector pinout (front view)

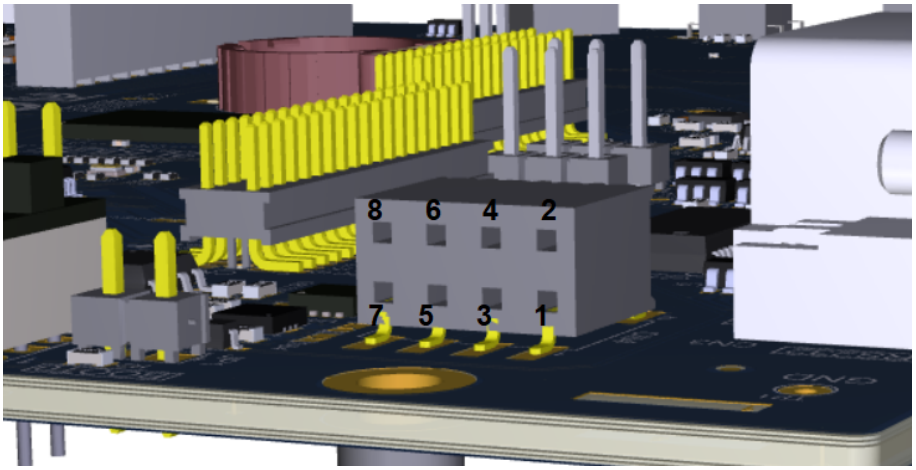


Table 46 describes the CN4 EXT_I2C connector pinout.

Table 46. CN4 EXT_I2C connector pinout

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
NC	NC	1	2	GND	GND
NC	NC	3	4	VDD	VDD
MFX_IO8	EXT_RESET	5	6	I2C1_SCL	PG14
NC	NC	7	8	I2C1_SDA	PG13

6.24 Touch-sensing button

The STM32L552E-EV Evaluation board supports a touch-sensing button based on either RC charging or on charge-transfer technique. This one is enabled by default.

6.24.1 Touch-sensing button I/O interface

The touch sensing button is connected to PC6 port of STM32L552ZET6QU and the related charge capacitor is connected to PC7.

An active shield is designed in layer 2 of the main PCB, under the button footprint. It allows reducing disturbances from other circuits to prevent false touch detections.

The active shield is connected to the PB6 port of STM32L552ZET6QU through the resistor R20. The related charge capacitor is connected to PB7.

The SB configuration related to the touch sensing function enables or disables its operation. However, most of them serve to optimize the touch sensing performance, by isolating copper tracks to avoid disturbances due to their antenna effect.

Table 47 describes the HW configuration for the touch-sensing button interface.

Table 47. HW configuration for the touch-sensing button interface

I/O	Resistor	Setting[1]	Configuration
PC6	SB11 SB12	ON	PC6 is connected to the I/O extension connector, thanks to SB12, or to the motor-control connector, thanks to SB11. The touch button TKEY function is not optimized.
		OFF	**PC6 is only connected to the touch button.** **PC6 can't be used for motor control and the I/O extension connector.**
PC7	SB2 SB3 SB5	ON	PC7 is connected to the I/O extension connector, thanks to SB5, or to the motor-control connector, thanks to SB2, or to the audio DFSDM interface, thanks to SB3. The touch button TKEY_CS function is not optimized.
		OFF	**PC7 is only connected to Touch Button** **PC7 can't be used for motor control, Audio DFSDM, STMOD+ or and I/O extension connector.**
PB6	SB15 SB17	ON	PB6 is connected to the I/O extension connector, thanks to SB17, or to the motor-control connector, thanks to SB15. The touch button SHIELD is not optimized.
		OFF	**PB6 is only connected to the touch button** **PB6 can't be used for motor control and the I/O extension connector.**
PB7	R229	**ON**	**PB7 is connected to the touch button SHIELD_CS.**
		OFF	PB7 is not connected to the touch button. No other muxing

1. *The default configuration is shown in bold.*

6.24.2 I/O restriction to other features

Caution: Due to the share of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the touch-sensing button features:

- The touch-sensing button cannot be operated simultaneously with the motor-control function.
- The touch-sensing button cannot be operated simultaneously with the external MEMS module.
- The touch-sensing button cannot be operated simultaneously with the STMPS2 for measurement using the Sigma Delta interface.
- The touch-sensing button cannot be operated simultaneously with the STMOD+.

6.25 MFX MCU

The MFX MCU, multi-function expander MCU, is used as GPIO-expander and IDD measurement U18.

6.25.1 Operating voltage

The MFX MCU is connected to VDD and is fully compatible with the MCU voltage range from 1.71 to 3.6 V.

6.25.2 MFX IO-expander

The MFX circuit on the STM32L552E-EV Evaluation board acts as IO-expander. The communication interface between MFX and STM32L552ZET6QU is an I^2C bus, with a Wake-UP pin and an INT pin.
Table 48 describes the HW configuration for the MFX interface.

Table 48. HW configuration for the MFX interface

I/O	Resistor	Setting(1)	Configuration
PA0	SB118	**ON**	**PA0 is connected to MFX as MFX_IRQ_OUT.**
		OFF	PA0 is NOT connected to MFX. PA0 can be used for OPAMP, STMOD+ or motor control.
PG9	SB87	**ON**	**PG9 is connected to MFX as MFX_WAKEUP.**
		OFF	PG9 is NOT connected to MFX. PG9 can be used for STMOD+ or motor control.
PG13	R282	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**

1. *The default configuration is shown in bold.*

Table 49 describes the I/O signals driven by the MFX.

Table 49. I/O signals driven by the MFX

Pin number	Pin name	Signal name	Function
18	GPIO0	JOY_SEL	B1 Joystick selection
19	GPIO1	JOY_DOWN	B1 Joystick down direction
20	GPIO2	JOY_LEFT	B1 Joystick left direction
39	GPIO3	JOY_RIGHT	B1 Joystick right direction
40	GPIO4	JOY_UP	B1 Joystick up direction
15	GPIO5	MEMS_LED	CN24 LED for Ext audio Module
16	GPIO6	SMARTCARD_OFF	U26 Smartcard OFF
17	GPIO7	SMARTCARD_RST	U26 Smartcard RESET
29	GPIO8	EXT_RESET	CN4 I^2C module RESET
30	GPIO9	SMARTCARD_CMDVCC	U26 Smartcard VCC cmd
31	GPIO10	SMARTCARD_3V/5V	U26 Smartcard 3V 5V selection
32	GPIO11	LED_YELLOW	LD6 LED yellow
33	GPIO12	LCD_RESET	CN18 LCD Reset
26	GPIO13	LED_ORANGE	LD7 LED Orange
27	GPIO14	STMOD+_RST	P2 STMOD+ Reset
28	GPIO15	AUDIO_RESETN	U30 Audio reset

6.25.3 IDD measurement

STM32L552ZET6QU has a built-in circuit allowing to measure its own current consumption (IDD) in Run and Low-power modes, except for Shutdown mode. It is strongly recommended that, the MCU supply voltage (VDD_MCU line) does not exceed 3.3 V. This is because there are components on STM32L552E-EV supplied from 3.3 V that communicate with the MCU through I/O ports. Voltage exceeding 3.3 V on the MCU output port may inject current into 3.3 V-supplied peripheric I/Os and false the MCU current-consumption measurement.

Table 50 shows the settings of the jumper associated with the IDD measurement on the board.

Table 50. Jumper associated with the IDD measurement on the board

HW	Setting(1)	Configuration
JP8	**JP8 [1-2]**	**STM32L552ZET6QU has a built-in circuit allowing to measure its own current consumption.**
	JP8 [2-3]	IDD measurement is not available, bypass mode only for STM32L552ZET6QU VDD_MCU power supply.

1. *The default configuration is shown in bold.*

6.25.4 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the MFX features:

- The MFX cannot be operated simultaneously with the OPAMP function.
- The MFX cannot be operated simultaneously with the STMOD+ function.
- The MFX cannot be operated simultaneously with the motor-control function.

6.26 Motor control

The CN2 connector is designed to receive a motor-control (MC) module.

6.26.1 Motor-control I/O interface

The motor-control I/O interface is not connected by default because it is too much IO-consuming.

Table 51 describes the assignment of the motor-control interface and the I/O function associated with the STM32L552ZET6QU.

Table 51. Motor-control terminal and I/O function assignment

CN2 motor-control connector		STM32L552ZET6QU microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling motor control
1	Emergency Stop	PB6	TIM8_BKIN2	-	Close SB15 Remove SB17 (I/O extension)
2	GND	-	GND	-	-
3	PWM_1H	PC6	TIM8_CH1	-	Close SB11 Remove SB12 (I/O extension)
4	GND	-	GND	-	-
5	PWM_1L	PA7	TIM8_CH1N	-	Close SB79 Remove R198 (Octo-SPI)
6	GND	-	GND	-	-
7	PWM_2H	PC7	TIM8_CH2	-	Close SB2 Open SB3 DFSDM STMOD+ Open SB5 (IO extension)

CN2 motor-control connector		STM32L552ZET6QU microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling motor control
8	GND	-	GND	-	-
9	PWM_2L	PB0	TIM8_CH2N	-	Close SB76 Remove R195 (Octo-SPI)
10	GND	-	GND	-	-
11	PWM_3H	PC8	TIM8_CH3	-	Close SB57 Open SB56 (SDIO)
12	GND	-	GND	-	-
13	PWM_3L	PB1	TIM8_CH3N	-	Close SB74 Remove R194 (Octo-SPI)
14	Bus Voltage	PA4	ADC12_IN9	-	Close SB122 Open SB107 UCPD Open SB108 STMOD+ or no daughterboard Open SB124 or no ADC/DAC on CN12
15	PhaseA current+	PC0	ADC12_IN1	-	Close SB90 Remove R209 (Octo-SPI)
16	PhaseA current-	-	GND	-	-
17	PhaseB current+	PC1	ADC12_IN2	-	Close SB91 Remove R215 (Octo-SPI)
18	PhaseB current-	-	GND	-	-
19	PhaseC current+	PC2	ADC12_IN3	-	Close SB94 Remove R214 (Octo-SPI)
20	PhaseC current-	-	GND	-	-
21	ICL Shutout	PG9	GPIO	-	Close SB85 Open SB87: MFX Open SB81 STMOD+
22	GND	-	GND	-	-
23	Dissipative Brake	PB2	GPIO	-	Close SB70 Remove R189 (Octo-SPI)
24	PFC indirect current	PC3	ADC12_IN4	-	Close SB100 Remove R218 (Octo-SPI)
25	5V	-	5V	-	-
26	Heatsink Temp.	PA3	ADC12_IN8	-	Close SB86 Removed R206 (Octo-SPI) Open SB84 OPAMP
27	PFC Sync	PF9	TIM15_CH1	-	Close SB95 Open SB98 Audio SAI
28	3V3	-	3V3	-	-
29	PFC PWM	PF10	TIM15_CH2	-	Close SB97 Open SB96 Audio DFSDM

CN2 motor-control connector		STM32L552ZET6QU microcontroller			
Terminal	Terminal name	Port name	Function	Alternate function	Board modifications for enabling motor control
30	PFC Shutdown	PA9	TIM15_BKIN	-	Close SB60 Open SB65 Smartcard
31	Encoder A	PA0	TIM2_CH1	ADC12_IN5	Close SB117 Open SB118 MFX Open SB116 OPAMP Open SB115 STMOD+
32	PFC Vac	PA6	ADC12_IN11	-	Close SB80 Remove R204 (Octo-SPI)
33	Encoder B	PA1	TIM2_CH2	ADC12_IN6	Close SB113 Open SB114 TAMPER KEY Open SB111 OPAMP Open SB112 STMOD+
34	Encoder Index	PA2	TIM2_CH3	ADC12_IN7	Close SB88 Removed R208 (Octo-SPI)

Figure 24 shows the CN2 motor-control connector pinout.

Figure 24. CN2 motor-control connector pinout

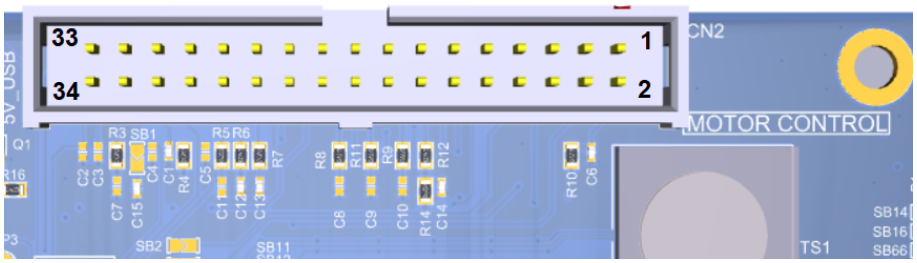


Table 52 describes the CN2 motor-control connector pinout.

Table 52. CN2 motor-control connector pinout

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
PB6	Emergency STOP	1	2	GND	-
PC6	PWM_1H	3	4	GND	-
PA7	PWM_1L	5	6	GND	-
PC7	PWM_2H	7	8	GND	-
PB0	PWM_2L	9	10	GND	-
PC8	PWM_3H	11	12	GND	-
PB1	PWM_3L	13	14	BUS VOLTAGE	PA4
PC0	CURRENT A	15	16	GND	-
PC1	CURRENT B	17	18	GND	-
PC2	CURRENT C	19	20	GND	-

STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin
PG9	ICL Shutout	21	22	GND	-
PB2	DISSIPATIVE BRAKE	23	24	PCD Ind. Current	PC3
-	+5V power	25	26	Heatsink temperature	PA3
PF9	PFC SYNC	27	28	3.3 V power	-
PF10	PFC PWM	29	30	PFC Shut Down	PA9
PA0	Encoder A	31	32	PFC Vac	PA6
PA1	Encoder B	33	34	Encoder Index	PA2

6.26.2 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the motor-control features:

- Motor control cannot be operated simultaneously with the touch-sensing button function.
- Motor control cannot be operated simultaneously with the Octo-SPI function.
- Motor control cannot be operated simultaneously with the STMOD+ function.
- Motor control cannot be operated simultaneously with the SDIO function.
- Motor control cannot be operated simultaneously with the UCPD function.
- Motor control cannot be operated simultaneously with the ADC/DAC function.
- Motor control cannot be operated simultaneously with the MFX function.
- Motor control cannot be operated simultaneously with the OPAMP function.
- Motor control cannot be operated simultaneously with the AUDIO function.
- Motor control cannot be operated simultaneously with the SMARTCARD function.
- Motor control cannot be operated simultaneously with the TAMPER KEY function.

6.27 CN5, CN6, CN8, and CN9 extension connectors

The CN5, CN6, CN8 and CN9 headers complement to give access to all GPIOs of the STM32L552ZET6QU microcontroller. In addition to GPIOs, the following signals and power supply lines are also routed on these connectors:

- GND
- 5V
- 3V3
- 5V_DC
- VDD
- RESETn
- Clock terminals PC14-OSC32_IN, PC15-OSC32_OUT, PH0-OSC_IN, PH1-OSC_OUT

CN5 and CN6 have two rows header of 19 pins, with 1.27 mm pitch and 2.54 mm row spacing.

CN8 and CN9 have two rows header of 17 pins, with 1.27 mm pitch and 2.54 mm row spacing. Mainly used for FMC interface access.

For extension modules, SAMTEC RSM-series and SAMTEC SMS-series can be recommended as SMD and through-hole receptacles, respectively.

Figure 25 shows the CN5 and CN6 connector pinouts.

Figure 25. CN5 and CN6 connector pinouts

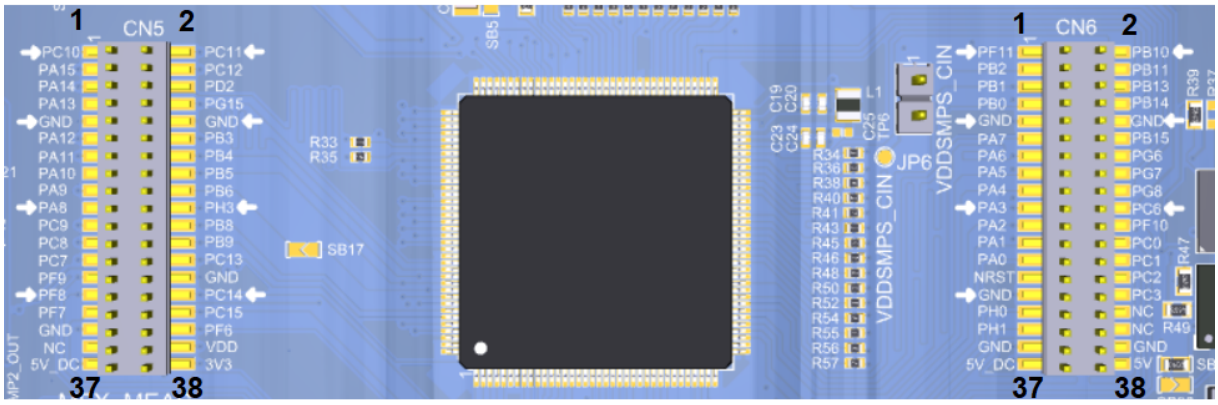


Table 53 describes the CN5 connector pinout.

Table 53. CN5 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PC10	SDIO, TRACE	1	2	SDIO	PC11
PA15	UCPD, TRACE	3	4	SDIO, SPI, TRACE	PC12
PA14	SWD	5	6	SDIO	PD2
PA13	SWD	7	8	LCD INT	PG15
GND	Power	9	10	Power	GND
PA12	USB_FS_P	11	12	LED, JTAG	PB3
PA11	USB_FS_N	13	14	JTAG, COMP, STMOD+	PB4
PA10	Audio_SAI	15	16	UCPD, COMP, STMOD+	PB5
PA9	Smartcard, motor control	17	18	Touch key, motor control	PB6
PA8	Smartcard	19	20	BOOT0	PH3
PC9	SDIO, TRACE	21	22	CAN FD	PB8
PC8	SDIO, motor control	23	24	CAN FD	PB9
PC7	Touch key, DFSDM, motor control	25	26	Wake-up key	PC13
PF9	Audio SAI, motor control	27	28	Power	GND
PF8	Audio SAI	29	30	OSC32_IN	PC14
PF7	Audio SAI	31	32	OSC32_OUT	PC15
GND	Power	33	34	Audio SAI	PF6
NC	NC	35	36	Power	VDD
5V_DC	Power	37	38	Power	3V3

Table 54 describes the CN6 connector pinout.

Table 54. CN6 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PF11	Octo-SPI	1	2	USART VCP, RS232	PB10
PB2	Octo-SPI, motor control	3	4	USART VCP, RS232	PB11
PB1	Octo-SPI, motor control	5	6	LPUART	PB13
PB0	Octo-SPI, motor control	7	8	UCPD	PB14
GND	Power	9	10	Power	GND
PA7	Octo-SPI, motor control	11	12	UCPD	PB15
PA6	Octo-SPI, motor control	13	14	LPUART	PG6
PA5	LCD_BL, STMOD+	15	16	LPUART VCP, RS232	PG7
PA4	UCPD, STMOD+, ADC/DAC, motor control	17	18	LPUART VCP, RS232	PG8
PA3	Octo-SPI, OPAMP, motor control	19	20	Touch key, motor control	PC6
PA2	Octo-SPI, motor control	21	22	DFSDM, motor control	PF10
PA1	Tamper key, OPAMP, STMOD +, motor control	23	24	Octo-SPI, motor control	PC0
PA0	MFX, OPAMP, STMOD+, motor control	25	26	Octo-SPI, motor control	PC1
NRST	RESET	27	28	Octo-SPI, motor control	PC2
GND	Power	29	30	Octo-SPI, motor control	PC3
PH0	OSC-IN	31	32	NC	NC
PH1	OSC_OUT	33	34	NC	NC
GND	Power	35	36	Power	GND
5V_DC	Power	37	38	Power	5V

Figure 26 shows the CN8 and CN9 connector pinouts.

Figure 26. CN8 and CN9 connector pinouts

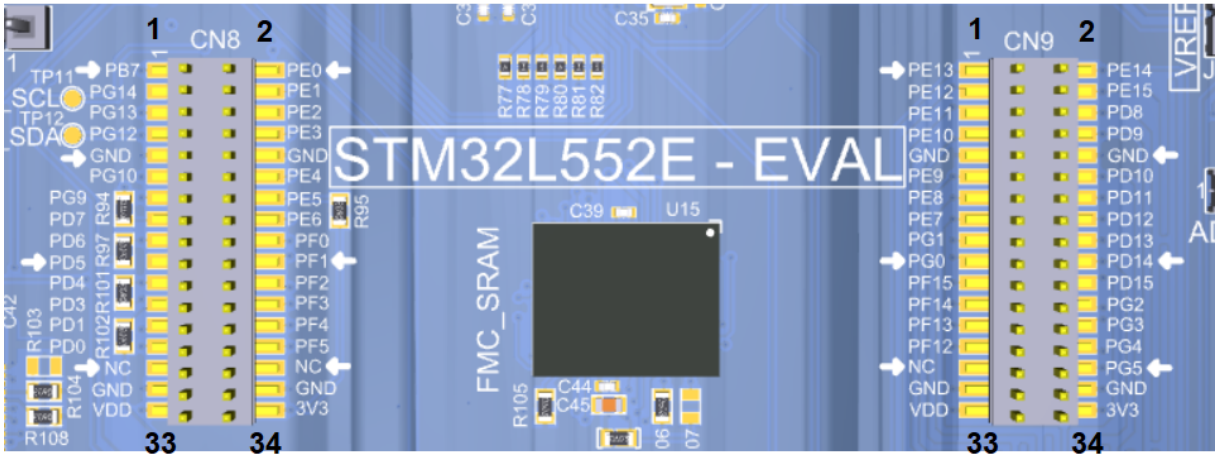


Table 55 describes the CN8 connector pinout.

Table 55. CN8 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PB7	Touch key	**1**	**2**	SRAM-FMC	PE0
PG14	I2C	**3**	**4**	SRAM-FMC	PE1
PG13	I2C	**5**	**6**	TRACE	PE2
PG12	LCD-FMC	**7**	**8**	SRAM-FMC	PE3
GND	Power	**9**	**10**	Power	GND
PG10	SDIO, STMOD+	**11**	**12**	SRAM-FMC	PE4
PG9	MFX, STMOD+, motor control	**13**	**14**	TRACE	PE5
PD7	SRAM-FMC	**15**	**16**	LCD-FMC	PE6
PD6	DFSDM	**17**	**18**	SRAM-FMC	PF0
PD5	LCD-SRAM-FMC	**19**	**20**	SRAM-FMC	PF1
PD4	LCD-SRAM-FMC	**21**	**22**	SRAM-FMC	PF2
PD3	LED	**23**	**24**	SRAM-FMC	PF3
PD1	LCD-SRAM-FMC	**25**	**26**	SRAM-FMC	PF4
PD0	LCD-SRAM-FMC	**27**	**28**	SRAM-FMC	PF5
NC	NC	**29**	**30**	NC	NC
GND	Power	**31**	**32**	Power	GND
VDD	Power	**33**	**34**	Power	3V3

Table 56 describes the CN9 connector pinout.

Table 56. CN9 connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PE13	LCD-SRAM-FMC	**1**	**2**	LCD-SRAM-FMC	PE14
PE12	LCD-SRAM-FMC	**3**	**4**	LCD-SRAM-FMC	PE15
PE11	LCD-SRAM-FMC	**5**	**6**	LCD-SRAM-FMC	PD8
PE10	LCD-SRAM-FMC	**7**	**8**	LCD-SRAM-FMC	PD9
GND	power	**9**	**10**	power	GND
PE9	LCD-SRAM-FMC	**11**	**12**	LCD-SRAM-FMC	PD10
PE8	LCD-SRAM-FMC	**13**	**14**	SRAM-FMC	PD11
PE7	LCD-SRAM-FMC	**15**	**16**	SRAM-FMC	PD12
PG1	SRAM-FMC	**17**	**18**	SRAM-FMC	PD13
PG0	SRAM-FMC	**19**	**20**	LCD-SRAM-FMC	PD14
PF15	SRAM-FMC	**21**	**22**	LCD-SRAM-FMC	PD15
PF14	SRAM-FMC	**23**	**24**	SRAM-FMC	PG2
PF13	SRAM-FMC	**25**	**26**	SRAM-FMC	PG3
PF12	SRAM-FMC	**27**	**28**	SRAM-FMC	PG4
NC	NC	**29**	**30**	SRAM-FMC	PG5
GND	Power	**31**	**32**	Power	GND
VDD	Power	**33**	**34**	Power	3V3

6.28 TFT LCD

The CN18 34-pin 2.54 mm pitch female connector is designed to connect the MB989 TFT LCD daughterboard supporting the FMC interface.

The LCD module is composed of the TFT LCD module supporting a resolution of 240(RGB) x 320 dots 262K color, and a touch panel feature driven by a Resistive Touch Screen controller.

6.28.1 Operating voltage

The new design of the LCD module MB989 revC is compatible with a voltage range from 1.65 to 3.3 V. So LCD is fully compatible with the MCU low voltage of 1.8 V.

6.28.2 LCD interface

Table 57 describes the HW configuration for the LCD interface.

Table 57. HW configuration for the LCD interface

I/O	HW	Setting[1]	Configuration
PG12	R231	**ON**	**PG12 is used as LCD_CSn_FMC_NE4 and connected to LCD.**
PD5	R239	**ON**	**PD5 is used as FMC_NWE and connected to LCD and SRAM.**
PD4	R101	**ON**	**PD4 is used as FMC_NOE and connected to LCD and SRAM.**
PE6	R236	**ON**	**PE6 is used as LCD_RS_FMC_A22 and connected to LCD.**
MFX-IO12	-	**ON**	**MFX_IO12 is used as LCD_RESET and connected to LCD.**
PD14	R23	**ON**	**PD14 is used as FMC_D0 and connected to SRAM and LCD.**
PD15	R22	**ON**	**PD15 is used as FMC_D1 and connected to SRAM and LCD.**
PD0	R33	**ON**	**PD0 is used as FMC_D2 and connected to SRAM and LCD.**
PD1	R35	**ON**	**PD1 is used as FMC_D3 and connected to SRAM and LCD.**
PE7	R48	**ON**	**PE7 is used as FMC_D4 and connected to SRAM and LCD.**
PE8	R46	**ON**	**PE8 is used as FMC_D5 and connected to SRAM and LCD.**
PE9	R45	**ON**	**PE9 is used as FMC_D6 and connected to SRAM and LCD.**
PE10	R43	**ON**	**PE10 is used as FMC_D7 and connected to SRAM and LCD.**
PE11	R41	**ON**	**PE11 is used as FMC_D8 and connected to SRAM and LCD.**
PE12	R40	**ON**	**PE12 is used as FMC_D9 and connected to SRAM and LCD.**
PE13	R38	**ON**	**PE13 is used as FMC_D10 and connected to SRAM and LCD.**
PE14	R36	**ON**	**PE14 is used as FMC_D11 and connected to SRAM and LCD.**
PE15	R34	**ON**	**PE15 is used as FMC_D12 and connected to SRAM and LCD.**
PD8	R29	**ON**	**PD8 is used as FMC_D13 and connected to SRAM and LCD.**
PD9	R28	**ON**	**PD9 is used as FMC_D14 and connected to SRAM and LCD.**
PD10	R27	**ON**	**PD10 is used as FMC_D15 and connected to SRAM and LCD.**
PA5	SB106	**ON**	**PA5 is used as LCD_BL_CTRL.**
	SB106	OFF	PA5 is not used as LCD_BL_CTRL. PA5 can be used for STMOD+ (SB105 ON).
PG15	R191	**ON**	**PG15 is used as LCD_INT for the touch panel.**
PG13	R232	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**

1. *The default configuration is shown in bold.*

Figure 27 shows the CN18 LCD connector pinout.

Figure 27. CN18 LCD connector pinout

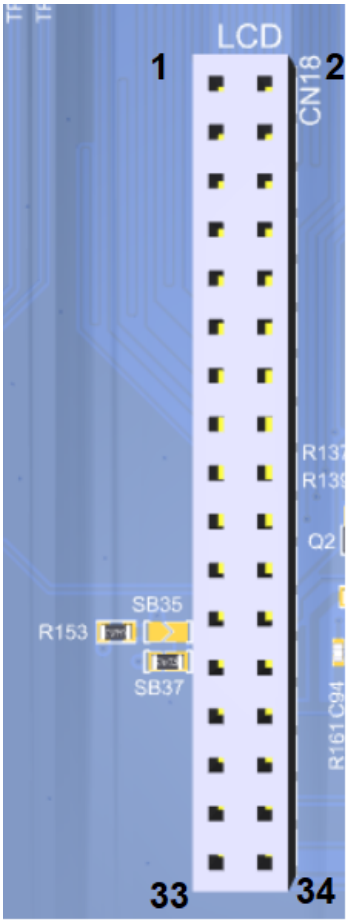


Table 58 describes the CN18 LCD interface and connector pinout.

Table 58. CN18 LCD connector pinout

STM32 pin	Board function	Pin	Pin	Board function	STM32 pin
PG12	LCD_CSn_FMC_NE4	1	2	LCD_RS_FMC_A22	PE6
PD5	FMC_NWE	3	4	FMC_NOE	PD4
MFX_IO12	LCD_RESET	5	6	D0	PD14
PD15	D1	7	8	D2	PD0
PD1	D3	9	10	D4	PE7
PE8	D5	11	12	D6	PE9
PE10	D7	13	14	D8	PE11
PE12	D9	15	16	D10	PE13
PE14	D11	17	18	D12	PE15
PD8	D13	19	20	D14	PD9
PD10	D15	21	22	BLGND	-
PA5	BL_CTRL	23	24	VDD_LCD	-
-	3V3	25	26	GND	-
-	GND	27	28	VDD_BL	-
-	-	29	30	GND	-
-	TSC_XL	31	32	TSC_XR	-
-	TSC_YD	33	34	TSC_YU	-

6.28.3 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the TFT features:

- The LCD BL_CTRL cannot be operated simultaneously with STMOD+ function. In this case, LCD backlight is forced to ON.
- FMC interface is shared with SRAM.

6.29 Pmod™ connector

The standard 12-pin Pmod™ connector is available on STM32L552E-EV Evaluation board to support low frequency, low I/O pin count peripherals module. The Pmod™ interface which is implemented on the STM32L552E-EV Evaluation board is compatible with the Pmod™ type 2A & 4A I/O signal assignment convention.

The Pmod™ connector supports several interface configurations:

- SPI interface: NSS, MOSI, MISO, SCK
- UART interface: TX, RX, CTS, RTS
- mikroBUS™ interface: NSS, TX, RX, SCK

In order to be able to support the selection of SPI or UART function connection on Pmod™, a quad SPDT switch is added on the board. This switch is controlled manually.

Table 59 describes the HW configuration for the Pmod™ interface.

Table 59. SW2 configuration for the Pmod™ interface

HW SW2 [1-2]	Interface
00	SPI interface selected
01	NOT USED
10	mikroBUS™ interface selected
11	UART interface selected

Table 60 describes the HW configuration for the Pmod™ interface.

Table 60. HW configuration for the Pmod™ interface

I/O	HW	Setting[1]	Configuration
PA4	SB108 / SB16	**ON/ON**	**PA4 is used as SPI_NSS on STMOD+.**
		OFF/ON	PA4 is not used as SPI_NSS on Pmod™ or STMOD+. PA4 can be used for USB or motor control or ADC/DAC.
PC12	SB62 / SB47	**ON/ON**	**PC12 is used as SPI3_MOSI on STMOD+.**
		OFF/ON	PC12 is not used as SPI3_MOSI on Pmod™ or STMOD+ PC12 can be used for SDIO or TRACE
PG10	SB52 / SB19	**ON/ON**	**PG10 is used as SPI3_MISO on STMOD+.**
		OFF/ON	PG10 is not used as SPI3_MISO on Pmod™ or STMOD+. PG10 can be used for SDIO
PG9	SB81 / SB69	**ON/ON**	**PG9 is used as SPI3_SCK on STMOD+.**
		OFF/ON	PG9 is not used as SPI3_SCK on Pmod™ or STMOD+. PG9 can be used for MFX or motor control.
PB13	R190 / SB14	**ON/ON**	**PB13 is used as LPUART1_CTS on STMOD+.**
		ON/OFF	PB13 is not used as LPUART1_CTS on Pmod™ or STMOD+ PB13 can be used for RS232.
PG7	SB49 / SB64	**ON/ON**	**PG7 is used as LPUART1_TX on STMOD+.**
		OFF/ON	PG7 is not used as LPUART1_TX on Pmod™ or STMOD+. PG7 can be used for T_VCP.
PG8	SB51 / SB18	**ON/ON**	**PG8 is used as LPUART1_RX on STMOD+.**
		OFF/ON	PG8 is not used as LPUART1_RX on Pmod™ or STMOD+. PG8 can be used for T_VCP.
PG6	R203 / SB66	**ON/ON**	**PG6 is used as LPUART1_RTS on STMOD+or for RS232.**
		ON/OFF	PG6 is not used as LPUART1_RTS on Pmod™. PG6 can be used for RS232 only.
PA1	SB112 / R186	**ON/ON**	**PA1 is used as PMOD_INT on Pmod™ shared with STMOD+.**
		OFF/ON	PA1 is not used as PMOD_INT on Pmod™ or STMOD+. PA1 can be used for TamperKey, or OPAMP, or motor control.
MFX_IO14	R185	**ON**	**MFX_IO14 is used as PMOD_RST on Pmod™ shared with STMOD+.** No other muxing

1. *The default configuration is shown in bold.*

Figure 28 shows the Pmod™ connector P1 pinout.

Figure 28. P1 Pmod™ connector pinout

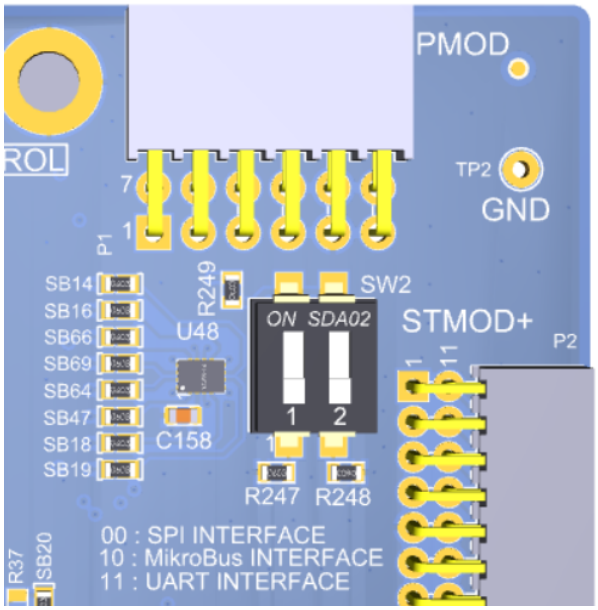


Table 61 describes the Pmod™ interface and connector P1 pinout.

Table 61. P1 Pmod™ connector pinout

Function	STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin	Function
SPI3 LPUART1	PA4 PB13	SPI_NSS LPUART1_CTS	1	7	PMOD_INT	PA1	INT1
SPI3 LPUART1	PC12 PG7	SPI3_MOSI UART_TX	2	8	PMOD_RST	MFX_IO14	Reset
SPI3 LPUART1	PG10 PG8	SPI3_MISO UART_RX	3	9	NC	NC	NC
SPI3 LPUART1	PG9 PG6	SPI3_SCK LPUART1_RTS	4	10	NC	NC	NC
GND	-	GND	5	11	GND	-	GND
Power	-	VDD	6	12	VDD	-	Power

6.29.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the Pmod™ features:

- The Pmod™ cannot be operated simultaneously with the STMOD+ function.
- The Pmod™ cannot be operated simultaneously with the UCPD function.
- The Pmod™ cannot be operated simultaneously with the ADC/DAC function.
- The Pmod™ cannot be operated simultaneously with the motor-control function.
- The Pmod™ cannot be operated simultaneously with the TRACE function.
- The Pmod™ cannot be operated simultaneously with the SDIO function.

- The Pmod™ cannot be operated simultaneously with the MFX function.
- The Pmod™ cannot be operated simultaneously with the RS-232 function.
- The Pmod™ cannot be operated simultaneously with the TAMPER KEY function.
- The Pmod™ cannot be operated simultaneously with the OPAMP function.

6.30 STMOD+ connector

The standard 20-pin STMOD+ connector is available on the STM32L552E-EV Evaluation board to increase compatibility with external boards and modules from the Ecosystem of microcontrollers. By default, it is designed to support an ST dedicated fanout board that allows connecting different modules or board extensions from different manufacturers. Fanout board also embeds a 3.3 V regulator and I^2C level shifter.

For all general information concerning the STM Fanout board MB1280, refer to STMOD+ interface specification (TN1238) at the *www.st.com* website.

The STMOD+ connector support several interface configurations:

- SPI interface: NSS, MOSI, MISO, SCK
- UART interface: TX, RX, CTS, RTS
- mikroBUS™ interface: NSS, TX, RX, SCK

In order to be able to support the selection of SPI or UART function connection on STMOD+, a quad SPDT switch is added on the board. This switch is controlled manually.

Table 62 describes the HW configuration for the STMOD+ interface.

Table 62. SW2 configuration for the STMOD+ interface

HW SW2 [1-2]	Interface
00	SPI interface selected
01	NOT USED
10	mikroBUS™ interface selected
11	UART interface selected

Table 63 describes the HW configuration for the STMOD+ interface.

Table 63. HW configuration for the STMOD+ interface

I/O	HW	Setting(1)	Configuration
PA4	SB108/SB16	**ON/ON**	**PA4 is used as SPI_NSS on STMOD+.**
		OFF/ON	PA4 is not used as SPI_NSS on Pmod™ or STMOD+. PA4 can be used for USB or motor control or ADC/DAC.
PC12	SB62/SB47	**ON/ON**	**PC12 is used as SPI3_MOSI on STMOD+.**
		OFF/ON	PC12 is not used as SPI3_MOSI on Pmod™ or STMOD+ PC12 can be used for SDIO or TRACE
PG10	SB52/SB19	**ON/ON**	**PG10 is used as SPI3_MISO on STMOD+.**
		OFF/ON	PG10 is not used as SPI3_MISO on Pmod™ or STMOD+. PG10 can be used for SDIO
PG9	SB81/SB69	**ON/ON**	**PG9 is used as SPI3_SCK on STMOD+.**
		OFF/ON	PG9 is Not used as SPI3_SCK on Pmod™ or STMOD+. PG9 can be used for MFX or motor control.

I/O	HW	Setting[1]	Configuration
PB13	R190/SB14	**ON/ON**	**PB13 is used as LPUART1_CTS on STMOD+.**
		ON/OFF	PB13 is Not used as LPUART1_CTS on Pmod™ or STMOD+ PB13 can be used for RS232.
PG7	SB49/SB64	**ON/ON**	**PG7 is used as LPUART1_TX on STMOD+.**
		OFF/ON	PG7 is Not used as LPUART1_TX on Pmod™ or STMOD+. PG7 can be used for T_VCP.
PG8	SB51/SB18	**ON/ON**	**PG8 is used as LPUART1_RX on STMOD+.**
		OFF/ON	PG8 is Not used as LPUART1_RX on Pmod™ or STMOD+. PG8 can be used for T_VCP.
PG6	R203/SB66	**ON/ON**	**PG6 is used as LPUART1_RTS on STMOD+or for RS232.**
		ON/OFF	PG6 is not used as LPUART1_RTS on PMOD. PG6 can be used for RS232 only.
PB5	SB99	**ON**	**PB5 is used as SPI3_MOSI2 on STMOD+.**
		OFF	PB5 is Not used as SPI3_MOSI2 on STMOD+. PB5 can be used for USB or COMP.
PB4	SB89	**ON**	**PB4 is used as SPI3_MISO2 on STMOD+.**
		OFF	PB4 is Not used as SPI3_MISO2 on STMOD+. PB4 can be used for JTAG or SDIO.
PG13	R232	**ON**	**PG13 is used as I2C1_SDA to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PG14	R228	**ON**	**PG14 is used as I2C1_SCL to interface the audio codec and it is shared with MFX, LCD, Ext_I2C, EEPROM, STMOD+.**
PA1	SB112/R186	**ON/ON**	**PA1 is used as PMOD_INT on Pmod™ shared with STMOD+.**
		OFF/ON	PA1 is Not used as PMOD_INT on Pmod™ or STMOD+. PA1 can be used for TamperKey, or OPAMP, or motor control.
MFX_IO14	R185	**ON**	**MFX_IO14 is used as PMOD_RST on Pmod™ shared with STMOD+.**
PA0	SB115	**ON**	**PA0 is used as ADC on STMOD+.**
		OFF	PA0 is Not used as ADC on STMOD+. PA0 can be used for MFX, OPAMP or motor control.
PA5	SB105	**ON**	**PA5 is used as PWM on STMOD+.**
		OFF	PA5 is Not used as PWM on STMOD+. PA5 can be used for LCD_BL_CTRL.
PD6	R97	**ON**	**PD6 is used as DFSDM_DATIN1 on STMOD+ shared with onboard MEMS, and the STMPS2 sensor.**
PF10	SB96	**ON**	**PF10 is used as DFSDM_CKOUT on STMOD+ shared with onboard MEMS, and STMPS2 sensor.**
		OFF	PF10 is Not used as DFSDM_CKOUT on STMOD+. PF10 can be used for motor control.
PC7	SB3	ON	PC7 is used as DFSDM_DATIN3 on STMOD+ shared with onboard MEMS.
		OFF	**PC7 is Not used as DFSDM_DATIN3 on STMOD+.** **PC7 can be used for Touch-Key or motor control.**

1. *The default configuration is shown in bold.*

Figure 29 shows the P2 STMOD+ connector pinout.

Figure 29. P2 STMOD+ connector pinout

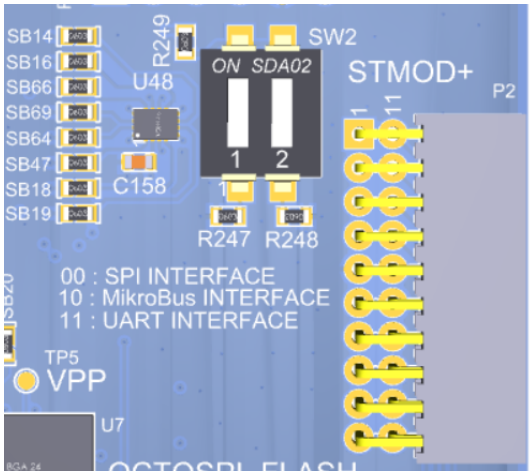


Table 64 describes the P2 STMOD+ interface and connector pinout.

Table 64. STMOD+ connector pinout

Function	STM32 pin	Signal name	Pin	Pin	Signal name	STM32 pin	Function
SPI3 LPUART1	PA4 PB13	SPI_NSS LPUART1_CTS	1	11	STMOD+_INT	PA1	INT1
SPI3 LPUART1	PC12 PG7	SPI3_MOSI UART_TX	2	12	STMOD+_RST	MFX_IO14	Reset
SPI3 LPUART1	PG10 PG8	SPI3_MISO UART_RX	3	13	STMOD+_ADC	PA0	ADC
SPI3 LPUART1	PG9 PG6	SPI3_SCK LPUART1_RTS	4	14	STMOD+_PWM	PA5	PWM
GND	-	GND	5	15	5V	-	Power
Power	-	5V	6	16	GND	-	GND
I2C1	PG14	I2C1_SCL	7	17	DFSDM1_DATIN1	PD6	DFSDM
SPI3	PB5	SPI3_MOSI2	8	18	DFSDM1_CKOUT	PF10	DFSDM
SPI3	PB4	SPI3_MISO2	9	19	DFSDM1_DATIN3	PC7	DFSDM
I2C1	PG13	I2C1_SDA	10	20	DFSDM1_CKOUT	PF10	DFSDM

6.30.1 I/O restriction to other features

Caution: Due to the sharing of some I/Os of STM32L552ZET6QU by multiple peripherals, the following limitations apply in using the STMOD+ features:

- The STMOD+ cannot be operated simultaneously with the PMOD function.
- The STMOD+ cannot be operated simultaneously with the UCPD function.
- The STMOD+ cannot be operated simultaneously with the ADC/DAC function.
- The STMOD+ cannot be operated simultaneously with the motor-control function.
- The STMOD+ cannot be operated simultaneously with the TRACE function.
- The STMOD+ cannot be operated simultaneously with the SDIO function.
- The STMOD+ cannot be operated simultaneously with the MFX function.
- The STMOD+ cannot be operated simultaneously with the RS-232 function.
- The STMOD+ cannot be operated simultaneously with the TAMPER KEY function.
- The STMOD+ cannot be operated simultaneously with the OPAMP function.
- The STMOD+ cannot be operated simultaneously with the LCD BL CTRL function.

7 Limitation

7.1 RSS/bootloader limitation

Issue observed:

The STM32L5 part soldered on STM32L552E-EV that embeds the bootloader V9.0 is affected by the limitations described in Section 6.9 RSS/bootloader.

Proposed workaround:

Refer to Section 6.9 RSS/bootloader to detail workaround.

Parts impacted:

This applies only to the STM32L552E-EV with the finished good (FG) **VAL552E$AU1** (Sticker available on the top side of the board).

7.2 SMPS limitation

Issue observed:

The STM32L5 part soldered on STM32L552E-EV embeds an internal SMPS. The sample revision rev B embeds two SMPS limitations: **SMPS regulation loss upon transiting into SMPS LP mode**, and **Unpredictable SMPS state at power-on**. Refer to errata sheet *STM32L552xx/562xx device errata* (ES0448) for more details.

Proposed workaround:

Refer to errata sheet *STM32L552xx/562xx device errata* (ES0448).

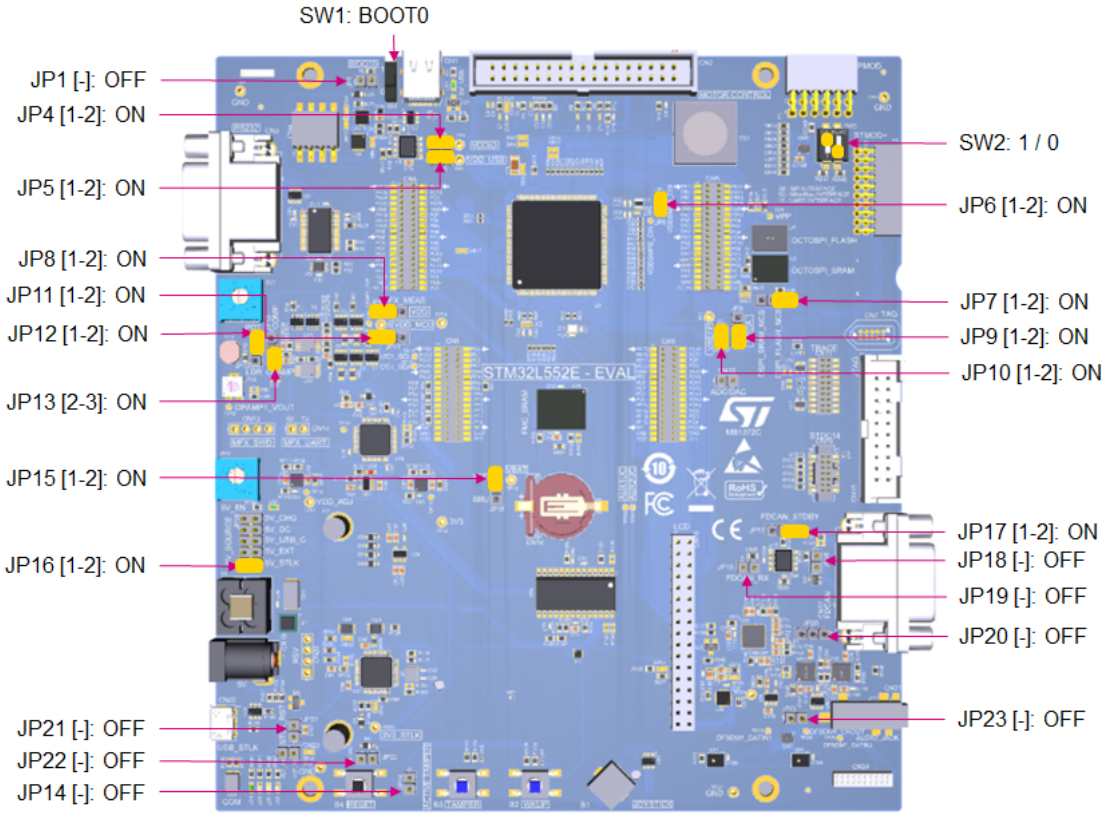
Parts impacted:

This applies only on the STM32L552E-EV with the finished good (FG) **VAL552E$AU1** (Sticker available on the top side of the board).

Appendix A STM32L552E-EV jumper summary

Figure 30 summarizes the jumper default setting of STM32L552E-EV.

Figure 30. Jumper default setting of STM32L552E-EV



Appendix B STM32L552E-EV I/O Assignment

Table 65. **STM32L552E-EV I/O Assignment**

LQFP144 pinout	Pin name	Main function pinout assignment	Optional function pinout assignment	Motor-control connector
1	PE2	TRACE_CLK	-	-
2	PE3	SRAM-FMC_A19	-	-
3	PE4	SRAM-FMC_A20	-	-
4	PE5	TRACE_D2	-	-
5	PE6	LCD_RS_FMC_A22	TRACE_D3	-
6	VBAT	POWER	-	-
7	PC13	User Button WKUP2	TAMPER KEY	-
8	PC14	OSC32_IN	-	-
9	PC15	OSC32_OUT	-	-
10	PF0	SRAM-FMC_A0	-	-
11	PF1	SRAM-FMC_A1	-	-
12	PF2	SRAM-FMC_A2	-	-
13	PF3	SRAM-FMC_A3	-	-
14	PF4	SRAM-FMC_A4	-	-
15	PF5	SRAM-FMC_A5	-	-
16	VSS	POWER	-	-
17	VDD	POWER	-	-
18	PF6	Audio SAI1_SD_B	-	-
19	PF7	Audio SAI1_MCLK_B	-	-
20	PF8	Audio SAI1_SCK_B	-	-
21	PF9	Audio SAI1_FS_B	-	TIM15_CH1
22	PF10	DFSDM1_CKOUT	STMOD+ DFSDM	TIM15_CH2
23	PH0	OSC_IN	-	-
24	PH1	OSC_OUT	-	-
25	NRST	NRST	-	-
26	PC0	OCTOSPI_IO7	-	ADC12_IN1
27	PC1	OCTOSPI_IO4	-	ADC12_IN2
28	PC2	OCTOSPI_IO5	-	ADC12_IN3
29	PC3	OCTOSPI_IO6	-	ADC12_IN4
30	VSSA	POWER	-	-
31	VREFP	POWER	-	-
32	VDDA	POWER	-	-
33	PA0	MFX_IRQ_OUT	OPAMP1_VINP, STMOD+_ADC12_IN5	ADC12_IN5 TIM2_CH1
34	PA1	TAMPER KEY	OPAMP1_VINM STMOD+_PMOD_INT	ADC12_IN6 TIM2_CH2

LQFP144 pinout	Pin name	Main function pinout assignment	Optional function pinout assignment	Motor-control connector
35	PA2	OCTOSPI_NCS	-	ADC12_IN7 TIM2_CH3
36	PA3	OCTOSPI_CLK	OPAMP1_VOUT	ADC12_IN8
37	VSS	POWER	-	-
38	VDD	POWER	-	-
39	PA4	UCPD_ADC12_IN9	ADC12_IN9/DAC1_OUT1 STMOD+_SPI3_NSS PMOD_SPI3_NSS	ADC12_IN9
40	PA5	LCD_BL_CTRL TIM2_CH1	STMOD+_TIM2_CH1	-
41	PA6	OCTOSPI_IO3	-	ADC12_IN11
42	PA7	OCTOSPI_IO2	-	TIM8_CH1N
43	PB0	OCTOSPI_IO1	-	TIM8_CH2N
44	PB1	OCTOSPI_IO0	-	TIM8_CH3N
45	PB2	OCTOSPI_DQS	-	I/O
46	PF11	OCTOSPI_NCLK	-	-
47	PF12	SRAM-FMC_A6	-	-
48	VSS	POWER	-	-
49	VDD	POWER	-	-
50	PF13	SRAM-FMC_A7	-	-
51	PF14	SRAM-FMC_A8	-	-
52	PF15	SRAM-FMC_A9	-	-
53	PG0	SRAM-FMC_A10	-	-
54	PG1	SRAM-FMC_A11	-	-
55	PE7	LCD-SRAM-FMC_D4	-	-
56	PE8	LCD-SRAM-FMC_D5	-	-
57	PE9	LCD-SRAM-FMC_D6	-	-
58	VSS	POWER	-	-
59	VDD	POWER	-	-
60	PE10	LCD-SRAM-FMC_D7	-	-
61	PE11	LCD-SRAM-FMC_D8	-	-
62	PE12	LCD-SRAM-FMC_D9	-	-
63	PE13	LCD-SRAM-FMC_D10	-	-
64	PE14	LCD-SRAM-FMC_D11	-	-
65	PE15	LCD-SRAM-FMC_D12	-	-
66	PB10	VCP_USART3_TX	RS-232_UART_TX STMOD+ UART_TX PMOD_UART_TX	-
67	PB11	VCP_USART3_RX	RS-232_UART_RX STMOD+ UART_RX PMOD_UART_RX	-

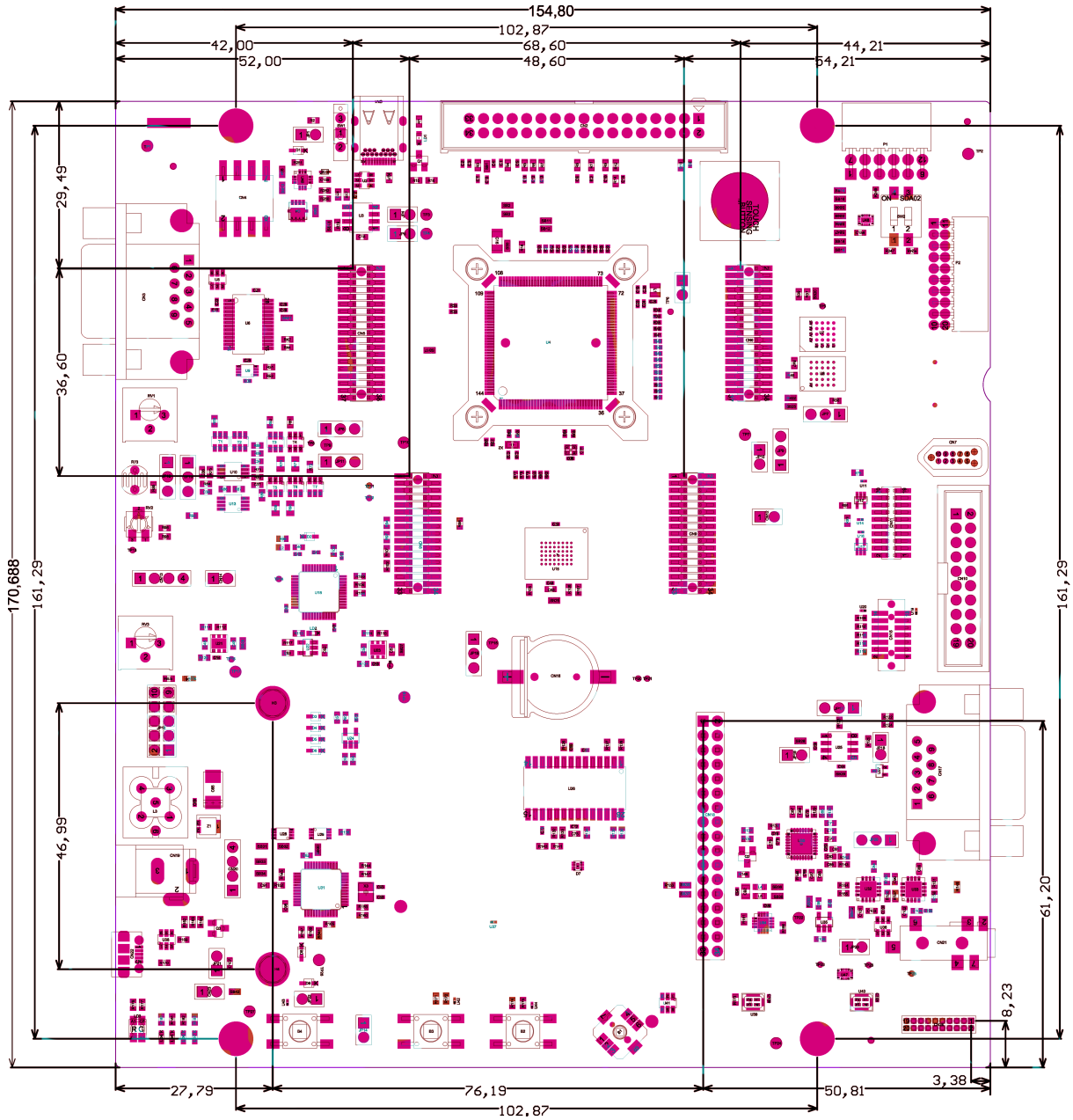
LQFP144 pinout	Pin name	Main function pinout assignment	Optional function pinout assignment	Motor-control connector
68	VDD_SMPS	POWER	-	-
69	VLX	POWER	-	-
70	VSS_SMPS	POWER	-	-
71	VSS	POWER	-	-
72	V15	POWER	-	-
73	VDD	POWER	-	-
74	PB13	RS232 LPUART1_CTS	STMOD+_LPUART1_CTS PMOD_LPUART1_CTS	-
75	PB14	UCPD_DB2	-	-
76	PB15	UCPD_CC2	-	-
77	PD8	LCD-SRAM-FMC_D13	-	-
78	PD9	LCD-SRAM-FMC_D14	-	-
79	PD10	LCD-SRAM-FMC_D15	-	-
80	PD11	SRAM-FMC_A16	-	-
81	PD12	SRAM-FMC_A17	-	-
82	PD13	SRAM-FMC_A18	-	-
83	VSS	POWER	-	-
84	VDD	POWER	-	-
85	PD14	LCD-SRAM-FMC_D0	-	-
86	PD15	LCD-SRAM-FMC_D1	-	-
87	PG2	SRAM-FMC_A12	-	-
88	PG3	SRAM-FMC_A13	-	-
89	PG4	SRAM-FMC_A14	-	-
90	PG5	SRAM-FMC_A15	-	-
91	PG6	RS232 LPUART1_RTS	STMOD+_LPUART1_RTS PMOD_LPUART1_RTS	-
92	PG7	RS232 LPUART1_TX	STMOD+_LPUART1_TX PMOD_LPUART1_TX VCP_LPUART1_TX	-
93	PG8	RS232 LPUART1_RX	STMOD+_LPUART1_RX PMOD_LPUART1_RX VCP_LPUART1_RX	-
94	VSS	POWER	-	-
95	VDD	POWER	-	-
96	PC6	-	Touch key	TIM8_CH1
97	PC7	DFSDM1_DATIN3	Touch key	TIM8_CH2
98	PC8	SDIO1_D0	-	TIM8_CH3
99	PC9	SDIO1_D1	TRACE_D0	-
100	PA8	Smartcard USART1_CK	-	-
101	PA9	Smartcard USART1_TX	-	TIM1_CH2

LQFP144 pinout	Pin name	Main function pinout assignment	Optional function pinout assignment	Motor-control connector
102	PA10	Audio SAI1_SD_A	-	-
103	PA11	USB_DM	-	-
104	PA12	USB_DP	-	-
105	PA13	SWDIO	JTAG_JTMS	-
106	VDDUSB	POWER	-	-
107	VSS	POWER	-	-
108	VDD	POWER	-	-
109	PA14	SWCLK	JTAG_JTCK	-
110	PA15	UCPD_CC	JTAG_JTDI	-
111	PC10	SDIO_D2	TRACE_D1	-
112	PC11	SDIO_D3	-	-
113	PC12	SDIO1_CK	STMOD+_SPI3_MOSI PMOD_SPI3_MOSI	-
114	PD0	LCD-SRAM-FMC_D2	-	-
115	PD1	LCD-SRAM-FMC_D3	-	-
116	PD2	SDIO1_CMD	-	-
117	PD3	LED_RED	-	-
118	PD4	LCD-SRAM-FMC_NOE	-	-
119	PD5	LCD-SRAM-FMC_NWE	-	-
120	VSS	POWER	-	-
121	VDD	POWER	-	-
122	PD6	DFSDM1_DATIN1	STMOD +_DFSDM1_DATIN1	-
123	PD7	SRAM-FMC_NE1	-	-
124	PG9	MFX_WAKE-UP	STMOD+_SPI3_SCK PMOD_SPI3_SCK	I/O
125	PG10	SDCARD_DETECT	STMOD+_SPI3_MISO PMOD_SPI3_MISO	-
126	PG12	LCD_CSn_FMC_NE4	-	-
127	PG13	I2C1_SDA	-	-
128	PG14	I2C1_SCL	-	-
129	VSS	POWER	-	-
130	VDD	POWER	-	-
131	PG15	LCD_CTP_INT	-	-
132	PB3	LED_GREEN	JTAG_JTDO_SWO	-
133	PB4	-	JTAG_NJTRST COMP2_INP STMOD+_SPI3_MISO2	-
134	PB5	UCPD_DB1	COMP2_OUT STMOD+_SPI3_MOSI2	-
135	PB6	-	Touch key	TIM8_BKIN2

LQFP144 pinout	Pin name	Main function pinout assignment	Optional function pinout assignment	Motor-control connector
136	PB7	-	Touch key	-
137	PH3	BOOT0	-	-
138	PB8	FDCAN1_RX	-	-
139	PB9	FDCAN1_TX	-	-
140	PE0	SRAM_FMC_NBL0	-	-
141	PE1	SRAM_FMC_NBL1	-	-
142	VSS	POWER	-	-
143	V15	POWER	-	-
144	VDD	POWER	-	-

Appendix C STM32L552E-EV mechanical drawing

Figure 31. **MB1372 STM32L552E-EV Evaluation board dimensions**



Appendix D Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

D.1 FCC Compliance Statement

Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

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Americas Region Legal | Group Vice President and Regional Legal Counsel, The Americas
STMicroelectronics, Inc.
750 Canyon Drive | Suite 300 | Coppell, Texas 75019
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Telephone: +1 972-466-7845

D.2 IC Compliance Statement

This device complies with FCC and Industry Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

Compliance Statement

Notice: This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'Industrie Canada: CAN ICES-3 (A) / NMB-3 (A).

D.3 Warning

EN 55032 / CISPR32 (2012) Class A product

Warning: this device is compliant with Class A of EN55032 / CISPR32. In a residential environment, this equipment may cause radio interference.

Avertissement : cet équipement est conforme à la Classe A de la EN55032 / CISPR 32. Dans un environnement résidentiel, cet équipement peut créer des interférences radio.

Revision history

Table 66. **Document revision history**

Date	Revision	Changes
28-Oct-2019	1	Initial release
28-Jan-2020	2	Added: • Section 7 Limitation Updated: • Section 6.9 RSS/bootloader

Contents

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