TLE986xQX BE

BootROM User Manual

Rev. 1.3, 2015-07-10

1 Introduction

This document specifies the BootROM firmware behaviors for the TLE986xQX family. The specification is organised into the following major sections:

- BootROM Overview
- Startup Procedure
- LIN and UART BSL features
- NVM structure and user routines description.

1.1 Purpose

The document describes the functionality of the BootROM firmware.

1.2 Scope

The BootROM firmware for the TLE986xQX family will provide the following features

- Startup procedure for stable operation of TLE986xQX chip
- Debugger connection for proper code debug
- BSL mode for users to download and run code from NVM and RAM
- NVM operation handling, e.g. program and erase

1.3Abbreviations and special terms

Table 1-1 Abbreviations and Terms

BSL	BootStrap Loader
CS	Configuration Sector
EOT	End of Transmission
EVR	Embedded Voltage Regulator
NAC	No Activity Count
NAD	Node address for diagnostic
NEA	NVM End Address
NLS	NVM Linear Size
NSA	NVM Starting Address
NVM	Non Volatile Memory
OCDS	On-Chip Debug Support
OSC	Oscillator
PEM	Program Execution Mode

Table 1-1 Abbreviations and Terms (cont'd)

PLL	Phase-Locked Loop
SA	Service Algorithm
SCU	System Control Unit
SWD	Serial Wire Debug
VTOR	Vector Table Offset Register
WDT	WatchDog Timer

2 Overview

This specification includes the description of all firmware features including the operations and tasks defined to support the general startup behaviour and various boot options.

2.1 Firmware architecture

TLE986xQX on-chip BootROM consists of the startup procedure, the bootstrap loader via LIN, the bootstrap loader via UART, NVM user routines and NVM integrity handling routines.

The BootROM in TLE986xQX is located at 00000000_H and so represents the standard reset handler routine.

The startup procedure includes the EVR calibration, MapRAM initialisation, on-chip oscillator configurations, NVM protection enabling and branching to the different modes. The deciding factor will be on the latched values of TMS, P0.0 and P0.2 upon a reset. During reset, these signals are latched at the rising edge of RESET pin and the latched values are used to define which operation mode has to be entered.

There are generally 2 operation modes in the BootROM:

- User / BSL mode
- Debug Support mode

For user mode, it will execute the startup procedure, set the vector table position at the beginning of the NVM in user accessible space (by proper setting of the VTOR register) and jump to the user defined reset handler routine (jump to the location pointed by the address 11000004_H-11000007_H) to execute the user program.

Note: The firmware will only set the VTOR to point at the beginning of the user accessible NVM region but will not write any vector table. This is the responsibility of the user to download a correct vector table.

Table 2-1 lists the boot options available in the TLE986xQX.

Table 2-1 TLE986xQX Boot options

TMS/DAP1	P0.0 /DAP0	P0.2	Mode / Comment
0	X	X	User mode / BSL mode [1)2)]
1	0	X	Device test mode[3)]
1	1	0	Debug mode with SWD port
1	1	1	Device test mode[3)]

1) On-chip OSC is selected as PLL input. System is running on LP_CLK until firmware switches to PLL output before jumping to user code. Exception is with hardware reset where user settings are retained.

2) Boot in user mode or BSL mode depends on the NAC word in user memory (NVM).

3) Power up with special internal settings. At completion, device runs in endless loop. No NVM code execution is performed.

Attention: The device test mode is not intended to be selected by the user. The user shall ensure by external configuration of the pins (TMS, P0.0 and P0.2) that no device test mode is entered.

2.2 Program structure

The different sections of the BootROM provide the following basic functionality.

Startup procedure

The startup procedure is the main control program in the BootROM. It is the first software controlled operation that is executed after any reset.

The startup procedure will perform configuration sector verification, EVR calibration, on-chip oscillator trimming, MapRAM initialisation, BootROM protection, NVM protection and decode the pin-latched values of the TMS, P0.0 and P0.2 to determine which mode it will jump to.

User mode

User mode is used to support user code execution in the NVM address space. However, if the NVM memories are not protected and the Bytes at address 11000004_H-11000007_H are erased (FF_H), then device enters sleep mode. If a valid user reset vector was found at 11000004_H (values at 11000004_H - 11000007_H not equal to $FFFFFFFF_H$) and a proper NAC value is found then the BootROM proceeds into user mode. In case an invalid NAC value is found, the device waits forever for a FastLIN BSL communication.

LIN BSL mode

It is used to support BSL via LIN like protocol. Downloading of code/data to RAM and NVM related programming is supported in this mode.

UART BSL mode

It is used to support BSL via UART protocol. Downloading of code/data to RAM and NVM related programming is supported in this mode.

3 Startup procedure

This chapter describes the BootROM startup procedure in TLE986xQX.

The startup procedure is the first software-controlled operation in the BootROM that is automatically started after every reset. Certain operations are skipped depending on the type of reset. Refer to next section for further details.

3.1 Program structure

The first task executed by the startup firmware is the check of the reset source. For power on, brown-out reset or wake-up from sleep mode reset, RAM test (optional) and initialization (mandatory) are executed while they are skipped for the other resets.

In particular, the RAM test is always executed in case of power-on and brown-out reset. For wake up reset, instead, the memory test execution is controlled by the MBIST_EN bit in the SystemStartConfig register. The user can freely set the value of this bit and its value is kept over wake up reset. If the bit is set to 0, the RAM test is not performed on wake up. If the bit is set to 1 then the RAM test is performed even for wake up resets.

Firmware code uses part of the RAM for variable storage, literal pools and stack pointer. The startup code anyhow only uses specific RAM region (the first 1kB mapped from address 18000000_H *to* $180003FF_H$*), subset of the total available RAM address range. The remaining region, not used by the FW, can be used by the user to store values to be valid across reset for all reset sources different from* power on reset, brown out reset and wakeup reset*. For these 3 reset sources, either a RAM test or a RAM clear is executed thus destroying the previously stored values.*

After that, depending on the reset source, the firmware will do NVM protection, NVM MapRAM initialisation, on-chip oscillator trimming, PLL setting and analog module trimming. It will decode the pin-latched values of the TMS, P0.0 and P0.2 to determine which mode it will jump to.

If bootup mode is Debug Support mode, the WDT1 is disabled. For entry to user mode, the WDT1 remains active. Next, the firmware will wait for NVM module to be ready.

For software, or internal watchdog reset (triggered by the WDT in the SCU), the following steps are skipped:

- RAM test and initialisation
- NVM MapRAM initialisation and service algorithm
- Setting of oscillator and PLL and switching system clock input to PLL output
- Loading of analog modules trimming parameters from first 100TP page
- Loading of user configuration data from 100TP page into the RAM
- Clearing of NMI status before exit to user mode or Debug support mode

3.1.1 Test and initialisation of RAM

A functional test sequence is executed on the entire RAM after power on reset and brown out reset and can be executed after a wakeup reset (depending on the value stored in the System Startup Configuration register). The test consists of a linear write/read algorithm using alternating data. Once started, the firmware waits until the test is completed before checking the result and continuing accordingly the start up sequence.

In case an error is detected the device is set to loop endlessly with WDT1 enabled.

Anyhow, in case of power-on reset, brown-out reset or wake-up reset from sleep mode the start up procedure will continue with a complete RAM initialization by writing all the RAM to zero with proper ECC status.This is needed to prevent an ECC error during user code execution due to a write operation to an un-initialised location (with invalid ECC code). Afterwards the Firmware proceeds checking the NVM status.

Note: The test sequence on the entire RAM takes 350 µs while the initialization of the complete RAM takes 100 µs.

3.1.2 NVM initialisation routine

This routine will set the NVM protection according to the password in the configuration sector (refer to **Section 6.4.5** for further details on NVM protection and protection password).

3.1.3 NVM MapRAM initialisation

After every power on reset, brown out reset, pin reset or wakeup reset the system performs the MapRAM initialisation. This operation is triggered to restore the MapRAM content. In case during the initialisation at least one error is detected, the service algorithm routine is called to do the repair.

In case of mapping errors, the repair mechanism consists of erasing the wrong pages (either faulty or double mapped pages). The repair step then requires the right of modifying the NVM Data sector content, which can be in contrast to the NVM protection settings user has provided. To avoid any risk of unwanted data loss, the user can control via dedicated 100TP page parameter whether the SA is allowed to proceed to the repair step in case NVM password protection for NVM Data sector is installed.

Detailed description of the MapRAM initialization and repair step can be found at **Section 6.4.1**

3.1.4 Oscillator trimming and system clock selection

After every power on reset, brown out reset, pin reset or wakeup from sleep reset the system runs with an internal low precision clock (nominally 18 MHz). During the start up procedure, the internal oscillator and PLL are trimmed to a fixed standard value of 20 MHz. In order to reduce the boot time, the start up procedure continues to run with the low precision clock while the PLL is locking. System clock will be switched to PLL output before jumping to user or BSL mode in case of successful lock. In case the PLL does not lock the startup sequence proceeds further using the low precision clock as system clock.

Once user mode is entered, user is allowed to set the final desired frequency by proper register setting.

Note: **After every power on reset, brown out reset, pin reset or wakeup reset the user shall check whether the system is running on the low precision clock or on the PLL output reading the SYSCON0 register.**

3.1.5 Analog module trimming

In this routine, the trimming values of voltage regulators, LIN module, temperature sensor, bridge driver and other analog modules are read from the configuration sector and written into the respective SFR. For user mode or Debug Support mode, checksum on 100TP page is evaluated. In case of error, default values are used. Refer to **Table 6-11** for a list of user parameters in 100TP page.

3.1.6 User configuration data initialization

The firmware provides a routine to download data stored in user accessible configuration sector pages (100TP) during the startup flow. In particular, the routine copies a specified number of Bytes from a selected CS page (starting always from first Byte in the page) into the RAM (starting at a given address). The routine is by default disabled and can be enabled and controlled by proper programming of the Bytes stored in first 100TP page as described in the **Table 6-11**. This routine is not performed after a software or watchdog reset.

Relevant routine control parameters stored in the first 100TP page are:

- CS_USER_CAL_STARTUP_EN (offset=79_H): When set to $C3_H$ it enables the user data download from a 100TP page into the RAM during startup flow. All other values will be ignored and the routine will not be executed at startup.
- CS_USER_CAL_XADDH: (offset=$7A_H$): It defines the high Byte of the RAM starting address where to copy data downloaded from CS. This Byte is ignored if the routine is not enabled.

- CS_USER_CAL_XADDL: (offset=7B$_H$): It defines the low Byte of the RAM starting address where to copy data downloaded from CS. This Byte is ignored if the routine is not enabled.
- CS_USER_CAL_CS_PAGE: (offset=7C$_H$): It defines the CS page where data has to be downloaded from (refer to **Figure 6-2**). This Byte is ignored if the routine is not enabled.
- CS_USER_CAL_NUM: (offset=7D$_H$): It defines the number of Bytes to be downloaded starting from the first Byte of the selected CS page. This Byte is ignored if the routine is not enabled.

The RAM address where the user configuration data has to be copied to is stored as a 16-bit offset to the RAM start address (18000000$_H$). This offset is defined by the CS_USER_CAL_XADDL and CS_USER_CAL_XADDH parameters.

The routine has been developed to support downloading of the Customer_ID and the ADC calibration parameters stored at the beginning of the first 100TP page (see **Table 6-11**) into the RAM for an easy access but can be more generally used for all other CS user parameters. If the routine is enabled, firmware will copy the data from config sector into the RAM. Moreover, independent of startup setting, a similar routine is provided as NVM user routine (refer to **Section 6.3.6**).

3.1.7 Debug support mode entry

Entry to Debug support mode is determined by pin setting at power up.

In case NVM address 11000004$_H$-11000007$_H$ is not FFFFFFFF$_H$, the firmware code clears the RAM, waits for debugger to be connected, moves the VTOR to 11000000$_H$ and jumps to user code.

3.1.8 User mode and BSL mode entry

Entry to user mode is determined by the No Activity Count (NAC) value which is defined in the user code (refer to **Chapter 3.1.8.1**). After waiting the time defined by the current NAC value, the startup procedure sets the VTOR register to point to the beginning of the NVM (11000000$_H$) and jumps to the reset handler.

If NVM double Bit error occurs when reading the NAC value, the system goes into endless loop.

Before exiting to user mode, the system clock frequency is switched to PLL output previously set by default to 20 MHz. In case PLL has not locked within 1 ms, the CPU clock source LP_CLK (low precision clock running nominally at 18 MHz) will be used.

Note: User mode is entered jumping to the reset handler. This can happen directly from startup routine, after a waiting time for possible BSL communication, or as a result of BSL commands. In all these cases, jump to user mode will only occur either (1) when NVM is not protected and NVM content at 11000004$_H$-11000007$_H$ is not

FFFFFFFF$_H$ or (2) when NVM is protected. In all other cases, firmware will put the device in sleep mode.

3.1.8.1 NAC definition

The NAC value defines the time window after reset release in which the firmware is able to receive BSL connection messages. The bits 3 to 0 define the duration of the time window while the bits 6 and 7 of the NAC define which BSL interface is selected. Bit 5 and 4 are not used. If no BSL messages are received on the selected BSL interface during the NAC window and NAC time has expired the firmware code proceeds to user mode.

After ending the start up procedure, the program will detect any activities on the LIN/UART for a period of time, determined by (((NAC & 3F$_H$) -1$_H$) * 5) ms reduced by the time already spent to perform the start up procedure. When nothing is detected on the LIN/UART and (((NAC & 3F$_H$) -1$_H$) * 5) ms is passed from reset going high, the microcontroller will jump to user mode. If NAC is 1$_H$, 41$_H$, 81$_H$ or C1$_H$ the BSL window is closed, no BSL connection is possible and the user mode is entered without delay.

The maximum NAC value is restricted to C$_H$ as the first open WDT1 window is worst case 65 ms. In case a valid BSL command is detected during the BSL window the firmware suspends the counting of the WDT1 in order to avoid that requested BSL communication is broken by a WDT1 reset. The firmware will then re-enable the WDT1 before jumping to user code. If NAC is not valid, BootROM code will switch off the WDT1 and wait for a Fast LIN frame infinitely.

Table 3-1 gives an overview of the action of the microcontroller with respect to No Activity Count (NAC) values and the **Table 3-2** shows the selection of the BSL interface depending on the NAC bits 7 and 6.

Table 3-1 Type of action w.r.t. No Activity Count (NAC) values

NAC Value	Action
01_H, 41_H, 81_H, $C1_H$	0 ms delay. Jump to user mode immediately
02_H, 42_H, 82_H, $C2_H$	5 ms delay before jumping to user mode[1)]
03_H, 43_H, 83_H, $C3_H$	10 ms delay before jumping to user mode[1)]
04_H, 44_H, 84_H, $C4_H$	15 ms delay before jumping to user mode[1)]
05_H, 45_H, 85_H, $C5_H$	20 ms delay before jumping to user mode[1)]
06_H, 46_H, 86_H, $C6_H$	25 ms delay before jumping to user mode[1)]
07_H, 47_H, 87_H, $C7_H$	30 ms delay before jumping to user mode[1)]
08_H, 48_H, 88_H, $C8_H$	35 ms delay before jumping to user mode[1)]
09_H, 49_H, 89_H, $C9_H$	40 ms delay before jumping to user mode[1)]
$0A_H$, $4A_H$, $8A_H$, CA_H	45 ms delay before jumping to user mode[1)]
$0B_H$, $4B_H$, $8B_H$, CB_H	50 ms delay before jumping to user mode[1)]
$0C_H$, $4C_H$, $8C_H$, CC_H	55 ms delay before jumping to user mode[1)]
$0D_H$ - $3F_H$, 00_H	Wait forever for the first LIN frame
$4D_H$ - $7F_H$, 40_H, Invalid	Wait forever for the first FAST LIN frame
$8D_H$ - BF_H, 80_H	Wait forever for the first UART frame
CD_H - FF_H, $C0_H$	Wait forever for the first UART frame

1) If a LIN frame/UART frame is received within the delay period, the following actions occur; (1) the remaining delay is ignored, (2) it will not enter user mode anymore (3) it will process the LIN / UART frame accordingly

Table 3-2 BSL interface selection

NAC(7)	NAC(6)	Selected BSL interface
0	0	LIN BSL
0	1	FAST LIN BSL
1	X	UART BSL

Note: LIN BSL will no longer be supported in future revisions of this product. All the LIN BSL features will be supported by FastLIN BSL but with higher baudrate.

For each derivative, the NAC value is stored, together with the NAD value, in the last 4 Bytes of the linearly mapped NVM region. To ensure the parameter validity, the 2 parameters' actual values and their inverted values are checked. In case the stored value and inverted value are not consistent (value + inverted value + 1 not equal to 0)

the parameter is considered to be invalid and the default value is used: The BSL window will be open indefinitely and FastLIN is selected as BSL interface.

The **Table 3-3** shows the addresses for all the available family devices. In the table NSA stands for NVM Starting Address whose value is 11000000_H for all derivatives and NLS stands for NVM Linear Size, in Bytes, whose value is derivative dependent.

Table 3-3 NAC and NAD parameters details

Address	User Defined Value	Criteria / Range	Default
NSA+(NLS-4)$_H$	NAC	01_H - $0C_H$ for LIN BSL 81_H - $8C_H$ for UART BSL	$7F_H$
NSA+(NLS-3)$_H$	$\overline{\text{NAC}}$	1's complement	-
NSA+(NLS-2)$_H$	NAD (for LIN BSL only)	01_H - FF_H (00_H is reserved)	$7F_H$
NSA+(NLS-1)$_H$	$\overline{\text{NAD}}$ (for LIN BSL only)	1's complement	-

For NSA and NLS values refer to **Table 6-2**.

4 LIN BSL mode

Note: LIN BSL will no longer be supported in future revisions of this product. All the LIN BSL features will be supported by FastLIN BSL but with higher baudrate.

LIN BSL is a LIN like protocol based on LIN 2.0 but for security reasons the checksum is inverted for most of the supported modes. Standard LIN protocol can support a max. baud rate of 20 kBaud. In order to support higher baudrates, a FastLIN BSL protocol has been introduced. This is an enhanced feature implemented in TLE986xQX device that supports baud rates of 20 kBaud to 57.6 kBaud and 115.2 kBaud via integrated LIN transceiver using UART BSL protocol (See **Section 4.6**).

4.1 LIN BSL features

Features that are implemented include:

1. Re-synchronization to the transfer speed (baud rate) of the communication partner upon receiving every frame
2. Using Diagnostic Frame (Master Request and Slave Response)
3. Usage of user values (NAD and NAC) stored in uppermost linearly mapped NVM
4. Non standard LIN checksum (Programming checksum, see **Section 4.4.3.2**)
5. Fast LIN BSL using UART protocol on integrated LIN transceiver

4.2 LIN BSL mode overview

The LIN BSL mode consists of three functional phases described below:

- **Phase I**: To establish a connection with every frame (Master Request or Slave Response frame) received by automatically synchronizing to the transfer speed (baud rate) of the communication partner (host).
- **Phase II**: To execute the host specified command. In order to execute the commands, host needs to send a Master Request Header first, followed by a Command frame within the 8 byte payload of the Master Request Frame. The selected mode information is embedded in the Command frame.
- The possible modes are:
  - **Mode 0 (00_H)**: Transfer a user program from the host to RAM[1)]
  - **Mode 1 (01_H)**: Execute a user program in the RAM[2)]
  - **Mode 2 (02_H)**: Transfer a user program from the host to NVM[1)]
  - **Mode 3 (03_H)**: Execute a user program in the NVM[2)]
  - **Mode 4 (04_H)**: Erase NVM[1)]
  - **Mode 6 (06_H)**: NVM Protection mode enabling/disabling Scheme[2)]
  - **Mode 8 (08_H):** Transfer a user program from the host to RAM using classic LIN checksum[3)]
  - **Mode 9 (09_H)**: Execute a user program in the RAM using classic LIN checksum[4)]
  - **Mode A ($0A_H$)**: Get info (based on Option Byte)[1)]

LIN BSL supports Fast Programming through modes 0, 2 and 8 with the selection of Fast Programming Option. Refer to **Section 4.4.4.2** for more details.

- **Phase III**: To send microcontroller status to host. In order to receive the microcontroller status, host needs to send a Slave Response Header first.

Re-synchronization and setup of baud rate (Phase I) are done at all times (before Phases II and III). Thus, different baud rates can be supported. Phase II is entered when its Master Request Header is received, otherwise Phase III is entered (Slave Response Header). The Master Request Header has a Protected ID of $3C_H$ while the Slave Response Header has a Protected ID of $7D_H$. The Command and Response frames are identified as Diagnostic LIN frame which has a standard 8 data Byte structure.

Figure 4-1 shows the relationship between the PC host and the microcontroller for the 3 phases, while **Figure 4-2** shows the Master Request Header, Slave Response Header, Command and Response frames.

1) The microcontroller returns to the beginning of Phase I/II and waits for the next command from the host
2) LIN BSL and serial communication are terminated.
3) Similar to mode 0, mode 8 uses classic LIN checksum instead of Programming checksum.
4) Similar to mode 1, mode 9 uses classic LIN checksum instead of Programming checksum.

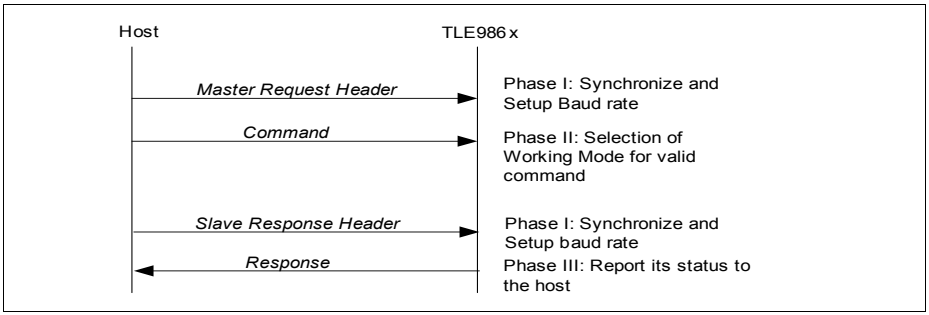

Figure 4-1 LIN mode - Phases I, II and III

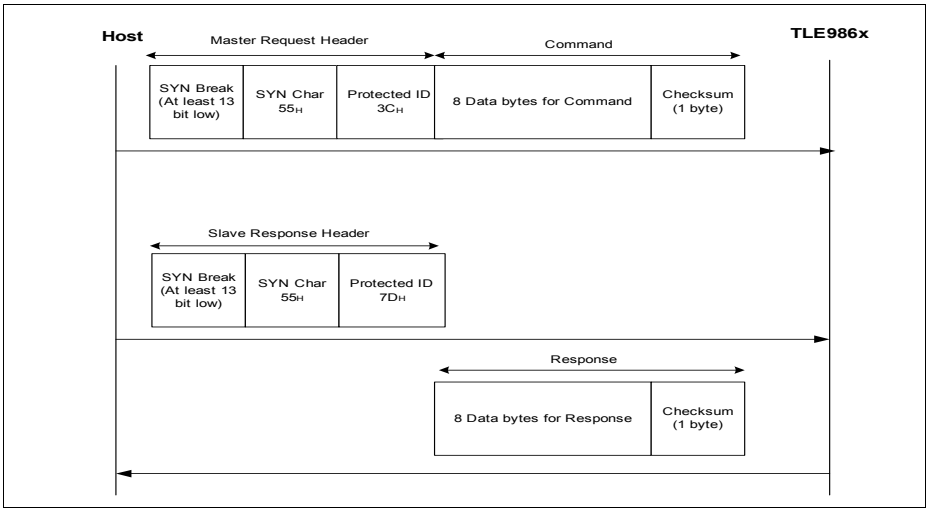

Figure 4-2 LIN mode - Frames

For all modes' entry, the Master Request Header is transmitted from host to microcontroller, followed by the command, which is the header block. The Slave Response Header is transmitted to check the status of the operation. For mode 0, 2 and 8, there is no need to send a Slave Response Header after every data block. The microcontroller supports multiple data block transfers (up to 256 data blocks) without Slave Response Headers in between, which saves overhead. As the commands are sent one after another without waiting for any status indication, a certain delay is required as shown in **Figure 4-3** to ensure sufficient time is provided for the microcontroller to execute the desired operations.

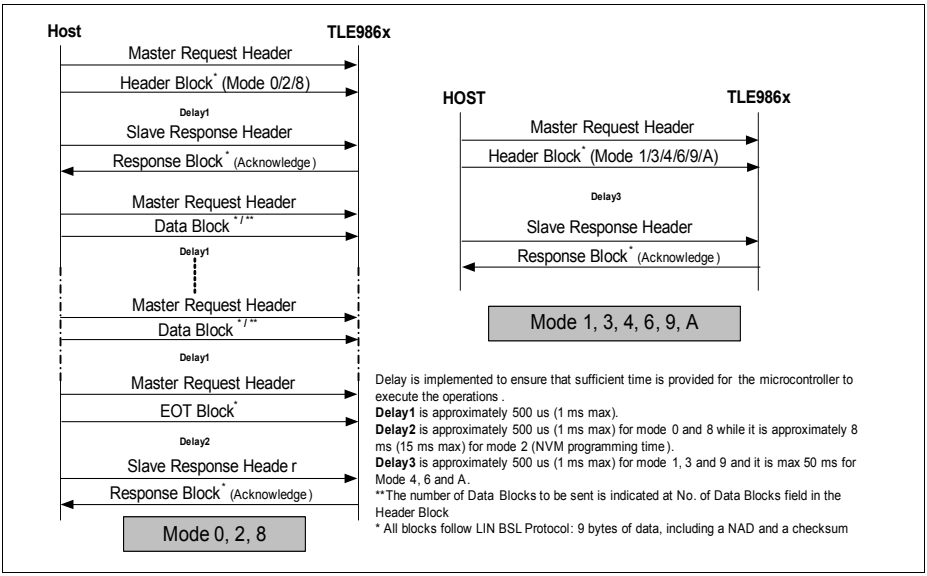

Figure 4-3 Communication structure of the LIN BSL modes

4.3 Phase I: Automatic synchronization to the host

Upon entry to LIN mode, a connection is established. The transfer speed (baud rate) of the device is automatically synchronized to the serial communication partner (host) in the following steps:

STEP 1: Initialize LIN interface for reception and timer 2 for baud rate measurement

STEP 2: Wait for an incoming frame from host

STEP 3: Synchronize the baud rate to the host

STEP 4: Enter Phase II (for Master Request Frame) or Phase III (for Slave Response Frame)

*Note: Re-synchronization and setup of baud rate are always done for **every** Master Request Header or Slave Response Header frame.*

4.3.1 General description

The LIN baud rate detection feature provides the capability to detect the baud rate within the LIN protocol using timer 2. Initialization consists of:

- Serial port of the microcontroller set to mode 1 (8-bit UART, variable baud rate) for communication

- baud rate range for detection, controlled by the field BGSEL of the BCON, set to “5.5 to 166.7 kBaud”.
- Capture Timer 2 data register contents on negative transition at pin T2EX
- Timer 2 external events are enabled (EXF2 flag is set when a negative transition occurs at pin T2EX)
- $f_{T2} = f_{PCLK} / 8$ (T2PRE = 011_B)

As shown in **Figure 4-2**, the LIN Header frame consists of the:

- synch Break (13 Bits time low)
- synch Byte (55_H)
- Protected ID field

The Break is used to signal the beginning of a new frame and must be at least 13 Bits of dominant value. When negative transition is detected at pin T2EX at the beginning of Break, the Timer 2 External Start Enable Bit (T2MOD.T2RHEN) is set. This will automatically start Timer 2 at the next negative transition of pin T2EX. Finally, the end of synch Byte flag (LINST.EOFSYN) is polled. When this flag is set, Timer 2 is stopped. T2 Reload/Capture register (RC2H/L) is the time taken for 8 Bits. Then the LIN routine calculates the actual baud rate, sets the PRE and BG values and activates baud Rate Generator. The baud rate detection for LIN is shown in **Figure 4-4**

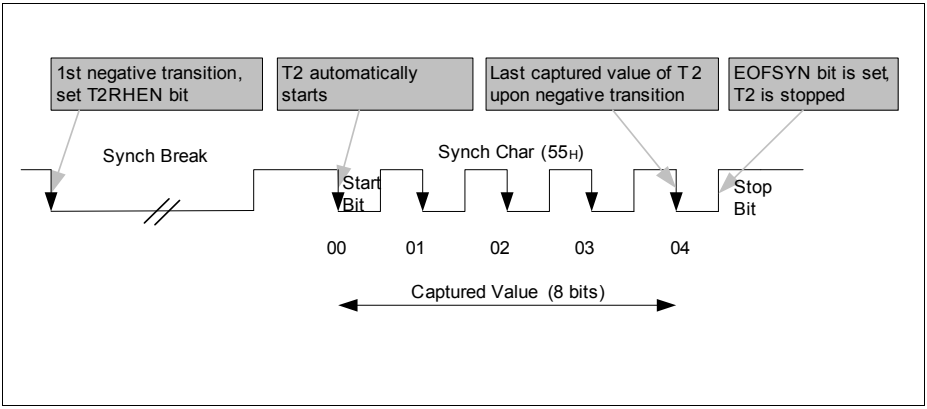

Figure 4-4 LIN autobaud rate detection

4.3.2 Calculation of BR_VALUE and PRE values

To set up auto baud rate detection, the BG and PRE values must be calculated. As there are two unknown values, two formulas are therefore needed. Firstly, the correlation between the baud rate (baud) and the reload value BR_VALUE (stored in the registers

BGL and BGH) and fractional divider (FDSEL) depends on the internal peripheral frequency (f_{PCLK}):

$$baud = \frac{f_{PCLK}}{16 \times PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right)} \quad [4.1]$$

Secondly, the relation between the baud rate (baud) and the captured value of Timer 2 (T2) depends on the T2 peripheral frequency (f_{T2}) and the number of received Bits (N_b):

$$baud = \frac{f_{T2} \times N_b}{T2} \quad [4.2]$$

Combining **Equation [4.1]** and **Equation [4.2]** with N_b=8, f_{T2}=f_{PCLK} / 8 (T2PRE=011_B) results in the following:

$$\frac{f_{PCLK}}{16 \times PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right)} = \frac{\frac{f_{PCLK}}{8} \times 8}{T2} \quad [4.3]$$

By simplifying **Equation [4.3]**, the following is obtained:

$$PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right) = \frac{T2}{16} \quad [4.4]$$

After setting BR_VALUE, PRE and FDSEL, the baud rate generator will then be enabled, and the subsequent Command frame or Response frame will follow this baud rate.

115.2 kBaud for FAST LIN

To support FAST LIN with baud rate 115.2 kBaud, fractional divider is enabled via a predefined factor calculated and stored in the configuration sector. The detection of 115.2 kBaud is determined by the T2 timing. If T2H and T2L is less than 154_H (i.e. baud rate roughly above 70 kBaud), baud rate will be set to 115.2 kBaud.

As a consequence, the settings for 115.2 kBaud are:

- BR_VALUE = 13 (SFR BGL.BR_VALUE = 101_B and SFR BGH = 1_H)
- PRE (SFR BCON.BRPRE) = 000_B
- Read FD_SEL value from configuration sector and store into SFR BGL. FD_SEL

4.4 Phase II: LIN BSL communication protocol and the working modes

Once successful synchronization to the host is completed (with a Master Request Header), the routine enters Phase II. Here, the host communicates to the microcontroller the desired working mode.

A simple protocol is defined for the communication between the host and TLE986xQX. The protocol data is performed in information blocks. The information block follows a specified block structure and is named transfer block. Each transfer block is 8 Bytes long plus 1 checksum Byte (required to be compliant to the LIN frame structure). A transfer block has the following structure:

NAD (1 byte)	Block Type (1 byte)	Data Area (6 bytes)	Checksum (1 byte)

- **NAD**: Node Address for Diagnostic, specifies the address of the active slave node. See **Section 4.4.1**.
- **Block Type**: This field determines the type of the message (See **Section 4.4.2**).
- **Data Area**: This is the data of the block. The length is fixed at 6 Bytes.
- **Checksum**: This checksum is calculated based on the NAD, Block Type and Data Area. See **Section 4.4.3**.

4.4.1 Node Address for Diagnostic (NAD)

The NAC value is stored similar to the NAC value inside the NVM. This field specifies the address of the active slave node. Only slave nodes have an address. The NAD address range supported in TLE986xQX is listed in **Table 4-1**.

Table 4-1 NAD address range

NAD Value	Description
00_H	Invalid Slave Address
$7F_H$	Default Address (NAD value is invalid or it is not programmed in NVM linear area)
01_H to $7E_H$ 80_H to FF_H	Valid Slave Address

Note: LIN block with Broadcast NAD ($7F_H$) is ignored if valid NAD value is programmed in NVM linear area.

*Note: For NAD address and details refer to **Table 3-3**.*

4.4.2 Block type

This field determines the types of transfer blocks. There are 3 transfer block types shown in **Table 4-2**.

Table 4-2 Type of transfer block

Block Name	Block Type	Description
Header block	00_H	Special information is contained in the data area of the block, which is used to select different working modes.
Data block	01_H	This block is used in working modes 0, 2 and 8 to transfer a portion of program code. The program code is in the data area of the block.
End of Transmission (EOT) block	02_H	This block is the last block in data transmission in working modes 0, 2 and 8. The last program code to be transferred is in the data area of the block.

4.4.3 Checksum

Diagnostic LIN frame always uses classic checksum where checksum calculation is over the data Bytes only. The Checksum is the last field of Command and Response LIN frames. For TLE986xQX, there are 2 types of checksum implemented, Classic (LIN) and Programming checksum. Both Programming and LIN Checksum are supported and are indicated in the respective modes.

4.4.3.1 Classic / LIN checksum

The classic checksum is a standard LIN checksum used for communication with LIN 2.0 slaves. The classic checksum contains the inverted eight Bits sum with carry[1)] over all data Bytes.

4.4.3.2 Programming checksum

The programming checksum, or Inverted Classic checksum is a non-LIN standard checksum. This is implemented in TLE986xQX to allow other slaves (not in TLE986xQX BSL mode) on the LIN bus to ignore this Programming frame. The inversion of the classic checksum yields the programming checksum.

An example of the calculation of the Programming checksum is provided in **Table 4-3**. For this example, data of $4A_H$, 55_H, 93_H and $E5_H$ is considered. The calculated

1) the checksum is calculated summing all values (8-bit sum with carry) and subtracting 255 every time the sum is greater or equal to 256 (which is not the same as modulo-255 or modulo-256).

programming checksum is 19_H. The classic checksum is an inversion of the programming checksum value (i.e. $E6_H$).

Table 4-3 Programming checksum

Addition of data	HEX	Result	CARRY	Addition with CARRY
$4A_H$	$4A_H$	$4A_H$	0	$4A_H$
$(4A_H) + 55_H$	$9F_H$	$9F_H$	0	$9F_H$
$(9F_H) + 93_H$	0132_H	32_H	1	33_H
$(33_H) + E5_H$	0118_H	18_H	1	19_H

4.4.4 LIN BSL Modes

When Phase II is entered, TLE986xQX waits for the Command frame and the header block from the host containing indication about the desired mode to be selected.

4.4.4.1 The Header Block

The header block is always the first transfer block to be sent by the host during each data communication process. It contains the mode number and special information on the related mode (referred to as “Mode Data”). The general structure of a header block is shown below.

NAD (1 byte)	Block Type 00_H (Header Block)	Data Area		Checksum (1 byte)
		Mode (1 byte)	Mode Data (5 bytes)	

Description:

- **NAD:** Node Address for Diagnostic. See **Section 4.4.1**
- **Block Type 00_H:** The Block Type, which marks the block as a header block
- **Mode:** The mode to be selected. The implemented modes are covered in **Section 4.2**
- **Mode Data:** Five Bytes of special information to activate corresponding mode.
- **Checksum:** The programming or LIN checksum of the header block.

Note: Mode 8 and mode 9 support LIN checksum, while mode 0 - 4, 6, and A support Programming checksum.

4.4.4.2 Mode 0, 2 and 8 - Code/Data download to RAM or NVM

Mode 0, 2 and 8 are used to transfer a user program from host to microcontroller. Mode 0 and 8 allow RAM transfers, while mode 2 allows NVM transfers.

These modes are disabled in case NVM is protected by proper password and a protection error is returned.

The header block has the following structure:

The header block

NAD (1 byte)	00_H (Header Block)	$00_H/02_H/08_H$ (Mode 0/2/8)	Mode Data (5 bytes)					Checksum (1 byte)
			Start Addr 3 (MSB)	Start Addr 2	Start Addr 1 (LSB)	No of Data Blocks Used (1 byte)	Fast_ Prog (1 byte)	

Mode Data Description:

Start Addr High, Low: 24-bit Start Address, which determines where to copy the received program codes in the RAM/NVM[1].

No. of data blocks used: Total number of data blocks to be sent, maximum 255 (FF_H) for mode 0 and 8 and maximum 21 (15_H) for mode 2. Consistency between number of data blocks declared in the header block and data blocks actually received is verified when EOT block is received. If numbers do not match, microcontroller will send a Block Type Error. PC host will then have to re-send the whole series of blocks (header, data and EOT blocks).

Fast_Prog: Indication Byte to enter Fast LIN BSL[2]

- 01_H: Enter Fast LIN BSL
- Other values: Ignored. Fast LIN BSL is not entered.

Note: The programming of NVM in mode 2 will be started after 128 Bytes or EOT are received. All Bytes sent during the program operation will be lost.

The start address provided with the header block has to be considered as a 24-bit offset to be added to the standard RAM (18000000_H) or NVM (11000000_H) base address. For mode 0 and 8, the most significant Byte of the start address is ignored.

When this Command frame (header block) is used for entering Fast LIN BSL, no other Master Request Header and Command frames (for data block or EOT block) should be sent. Instead, the microcontroller expects a Slave Response Header frame and sends a Response frame to Acknowledge receiving correct header block to enter Fast LIN BSL where UART BSL protocol is used. See **Section 4.6**

On successful receipt of the header block, the microcontroller enters mode 0/2/8, whereby the program code is transmitted from the host to the microcontroller by data block and EOT block, which are described below.

1) NVM address should be aligned to the Page address (low Byte of the start address equal to 00_H or 80_H). If the data starts in a non-page address, PC host should fill up the beginning vacancies with 00_H and provide the start address of that page address.
2) In the case NVM is protected, entry to FastLIN BSL is not possible.

The data block

NAD (1 byte)	01_H (Data Block 1 byte)	Data Area (6 bytes)	Checksum (1 byte)
		Program Code (6 bytes)	

Data area Description:

Program Code: The program code has a fixed length of 6 Bytes per data block.

The EOT block

NAD (1 byte)	02_H (EOT Block 1 byte)	Data Area (6 bytes)			Checksum (1 byte)
		Last_Code length (1 byte)	Program Code (Last_Codelength bytes)	Not Used (6-1-Last_Codelength bytes)	

Data area Description:

Last_Codelength: This Byte indicates the length of the program code in this EOT block.

Program Code: The last program code (valid data) to be sent to the microcontroller.

Not used: The length is (6 - 1 - Last_Codelength). These Bytes are not used and they can be set to any value.

Note:

1. *NVM programming needs to be performed in multiples of a page, 1 page is 128 Bytes. Host is expected to introduce a delay of 15 ms after 128 Bytes of program code are sent. Refer to example given below on mode 2 downloading.*
2. *To prevent external access, once the NVM is protected, modes 0, 2 and 8 are not accessible.*

Table 4-4 Example for 200 Bytes downloading using mode 0/8 and mode 2

Mode 0/8 - (RAM download)	Mode 2 - (NVM download)
Send Master Request Header	Send Master Request Header
Send header block • No of data blocks used = 33 • Start address (e.g. 000000_H)	Send header block • No of data blocks used = 21 • Start address (e.g. 000100_H)
Delay	Delay
Send Slave Response Header	Send Slave Response Header
Check for Acknowledge	Check for Acknowledge
Send 33 times (Master Request Header + data blocks) (Delay after each data block required)	Send 21 times (Master Request Header + data blocks) (Delay after each data block required)
Send Master Request Header	Send Master Request Header
Send EOT block • Last_Codelength = 2	Send EOT Block • Last_Codelength = 2
Delay	Delay
Send Slave Response Header	Send Slave Response Header
Check for Acknowledge	Check for Acknowledge
	Send Master Request Header
	Send header block • No of data blocks used = 12 • Start address (e.g. 000180_H)
	Delay
	Send Slave Response Header
	Check for Acknowledge
	Send 12 times (Master Request Header + data blocks) (Delay after each data block required)
	Send Master Request Header
	Send EOT block • Last_Codelength = 0
	Delay
	Send Slave Response Header
	Check for Acknowledge

33 blocks * 6 Bytes + 2 Bytes = 200 Bytes

4.4.4.3 Mode 1, 3 and 9 - Code execution inside RAM or NVM

Mode 1, 3 and 9 are used to trigger execution of a user program by the microcontroller. Mode 1 and 9 set the vector table in the RAM at the address 18000400_H and trigger execution of user program branching at address pointed by the standard reset handler (18000404_H). Mode 3 sets the vector table in the NVM at the address 11000000_H and triggers execution of user program branching at address pointed by the standard reset handler (11000004_H).The header block for this working mode has the following structure:

The header block

NAD (1 byte)	00_H (Header Block)	$01_H/03_H/09_H$ (Mode 1/3/9)	Mode Data	Checksum (1 byte)
			Not Used (5 bytes)	

Mode Data Description:

Not used: The five Bytes are not used and will be ignored in mode 1/3/9.

For modes 1, 3 and 9, the header block is the only transfer block to be sent by the host followed by a Slave Response Header. The microcontroller will send a response block (Acknowledgement code, 55_H), exit the LIN BSL and jump to the RAM at the address pointed by 18000404_H (mode 1 and mode 9) or jump to NVM address at the address pointed by 11000004_H (mode 3) respectively.

Note: For mode 3, jump to NVM will only occur either (1) when NVM is not protected and NVM content at 11000004_H is not FF_H or (2) when NVM is protected. In all other cases, firmware will put the device in sleep mode.

4.4.4.4 Mode 4 - NVM erase

Mode 4 is used to erase the NVM. 3 different options are supported:

- Option 00_H: Page Erase
- Option 40_H: Sector Erase
- Option $C0_H$: Mass Erase

The header block for Option = 00_H has the following structure:

The header block for page erase (Option = 00_H)

NAD (1 byte)	00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)					Checksum (1 byte)
			Start Addr 4 (MSB)	Start Addr 3	Start Addr 2	Start Addr 1 (LSB)	Option = 00_H (1 byte)	

Mode Data Description:

Start Addr 4 to 1: 32-bit address of the NVM page to be erased.

Option: set to 00_H to enable page erase.

When the Option Byte is 00_H, the NVM page selected by the address provided in the Mode Data field is erased. The address should be aligned with the beginning of the chosen page.

The header block for sector erase (Option = 40_H)

The header block for Option = 40_H has the following structure:

NAD (1 byte)	00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)					Checksum (1 byte)
			Start Addr 4 (MSB)	Start Addr 3	Start Addr 2	Start Addr 1 (LSB)	Option = 40_H (1 byte)	

Mode Data Description:

Start Addr 4 to 1: 32-bit address of the NVM sector to be erased.

Option: set to 40_H to enable sector erase.

When the Option Byte = 40_H, the NVM sector selected by the address provided in the Mode Data field is erased. The address should be aligned with the beginning of the chosen sector.

The Header for mass erase (Option = $C0_H$)

The header block for Option = $C0_H$ has the following structure:

NAD (1 byte)	00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)		Checksum (1 byte)
			Not Used (4 bytes)	Option = $C0_H$ (1 byte)	

Mode Data Description:

Not used: This Byte is not used and will be ignored in mode 4.

Option: set to $C0_H$ to enable mass erase.

When the Option Byte = $C0_H$, mass erase on all the sectors in the NVM unit is performed.

Note: When NVM is protected, mode 4 is not accessible and so NVM cannot be erased.

4.4.4.5 Mode 6 - NVM protection

Mode 6 is used to enable or disable the NVM protection mode (read and write protection of the Linearly and Non-Linearly mapped sectors) via the given user-password. The header block for this working mode has the following structure:

The header block

NAD (1 byte)	**00_H** (Header Block)	**06_H** (Mode 6)	**Mode Data** (5 bytes)		**Checksum** (1 byte)
			User-password (1 byte)	**Not Used** (4 bytes)	

Mode Data Description

User-password: This Byte is given by user to enable or disable NVM protection mode.

Not used: The four Bytes are not used and will be ignored in mode 6.

In mode 6, the header block is the only transfer block to be sent by the host. If device is unprotected, the provided user-password will be set as NVM_PASSWORD and internally stored. No further commands will be accepted until a power up or hardware reset. Afterwards, protection mode will be enabled.

However, if the NVM is already protected, the microcontroller will deactivate the Protection and erase the NVM if the user-password Byte matches the stored NVM_PASSWORD Byte. If MSB of the NVM_PASSWORD is 0, only NVM Linearly mapped sectors are erased. If the Bit is 1, both NVM Linearly and Non-linearly mapped regions are erased. No further commands will be accepted until a power up or hardware reset. Afterwards, protection mode will be disabled.

In case NVM is protected and the given user-password does not match the stored NVM_PASSWORD, no actions will be triggered and a Protection Error Byte will be returned instead of Acknowledge.

Note:

1. *Password value has to be different from 00_H and FF_H. In case on an unprotected device User-password is set to either 00_H or FF_H the protection will not be set and a protection error (FD_H) will be returned.*

2. *When disabling NVM protection, together with NVM, the NAC and NAD values are erased too. As a result, after next reset, default NAD will be used and chip waits forever in FastLIN mode with 115.2 kBaud.*

4.4.4.6 Mode A - Chip ID/Checksum read out

Mode A is used to get 4 Bytes Chip ID data, NVM page or CS page or mass NVM checksum check info depending on the Option Byte value in the header block. The header block for this mode has the following structure:

NAD (1 byte)	**00_H** (Header Block)	**$0A_H$** (Mode A)	**Mode Data** (5 bytes)		**Checksum** (1 byte)
			Input Data bytes (4 bytes)	**Option** (1 byte)	

Different options are supported:

- Option 00_H: Get 4 Bytes Chip ID
- Option 10_H: NVM page checksum check
- Option 18_H: Mass NVM checksum check
- Option 50_H: Configuration sector page checksum check

The header block - Get 4 Bytes Chip ID (Option = 00_H)

The header block for Option = 00_H has the following structure:

NAD (1 byte)	**00_H** (Header Block)	**$0A_H$** (Mode A)	**Mode Data** (5 bytes)		**Checksum** (1 byte)
			Not Used (4 bytes)	Option = 00_H (1 byte)	

Mode Data Description:

Not used: These Bytes are not used and will be ignored.

Option: set to 00_H to enable getting 4 Bytes Chip ID info.

When the Option Byte = 00_H, the 4 Byte Chip ID Number will be returned (see **Chapter 4.5.3**).

The header block - NVM page checksum check (Option = 10_H)

The header block for Option = 10_H has the following structure:

NAD (1 byte)	00_H (Header Block)	$0A_H$ (Mode A)	Mode Data (5 bytes)					Checksum (1 byte)
			Start Addr High (1 byte)	Start Addr Low (1 byte)	Exp CHKS High (1 byte)	Exp CHKS Low (1 byte)	Option = 10_H (1 byte)	

Mode Data Description:

Start Addr High, Low: Address of the NVM page for checksum check. (Address should be page aligned).

Exp. CHKS High, Low: Expected checksum High/Low Byte.

Option: set to 10_H to enable NVM page checksum check.

Note: The start address provided with the header block has to be shifted by 7 bits to the left and then added to the NVM start address to build the actual address, i.e. it is calculated as follows in Mode A Option 10_H: Actual address = 11000000_H + (StartAddrHigh << 15) + (StartAddrLow << 7).

This option will trigger a checksum calculation (16 bits inverted XOR) over the whole page pointed by the address calculated form the offset provided in the header block and the result will then be compared with the expected checksum (provided as well by the user in the header frame). The response frame will then return an Acknowledge followed by four data Bytes. These Bytes are, in sequential order, pass/fail indication (00_H if the calculated and expected checksum match, 80_H if they differ), calculated checksum High Byte, calculated checksum Low Byte, and a final Byte equal to 00_H.

In case the provided address is not a valid NVM address, the microcontroller will return a Block Type Error (FF_H) instead of an Acknowledge (55_H) followed by no further Bytes.

The header block - Mass NVM checksum check (Option = 18_H)

The header block for Option = 18_H has the following structure:

NAD (1 byte)	00_H (Header Block)	$0A_H$ (Mode A)	Mode Data (5 bytes)					Checksum (1 byte)
			Not Used (1 byte)	Not Used (1 byte)	Exp CHKS High (1 byte)	Exp CHKS Low (1 byte)	Option = 18_H (1 byte)	

Mode Data Description:

Not used: These Bytes are not used and will be ignored.

Exp. CHKS High, Low: Expected checksum High/Low Byte.

Option: set to 18_H to enable Mass NVM checksum check.

Checksum (16 Bits inverted XOR) on the whole linearly mapped sectors (configuration sector pages and non-linearly mapped sectors not included) is calculated and then compared with the expected values (provided as well as an input). The response frame will then give back a pass or fail indication plus the calculated checksum.

The header block - Configuration sector page checksum check (Option = 50_H)

The header block for Option = 50_H has the following structure:

NAD (1 byte)	**00_H** (Header Block)	**$0A_H$** (Mode A)	**Mode Data** (5 bytes)					**Checksum** (1 byte)
			CS Page (1 byte)	**Not Used** (1 byte)	**Exp CHKS High** (1 byte)	**Exp CKSum Low** (1 byte)	**Option** = 50_H (1 byte)	

Mode Data Description:

CS Page: Selection of the CS Page to be checked (refer to **Figure 6-2**).

Not used: This Byte is not used and will be ignored.

Exp. CHKS High, Low: Expected checksum High/Low Byte.

Option: set to 50_H to enable configuration sector page checksum check.

Checksum (16 Bits inverted XOR) on the selected configuration sector page is calculated and then compared with the expected values (provided as well as an input). The response frame will then give back a pass or fail indication plus the calculated checksum. In case the provided CS address is not valid, the microcontroller will return a Block Type Error (FF_H) followed by no further Bytes.

For mode A, the header block is the only transfer block to be sent by the host followed by a Slave Response Header. In case of valid header block, the microcontroller will send a response block (Acknowledgement code, 55_H) followed by the 4 Bytes data. The response for mode A is described in **Section 4.5.3**.

4.5 Phase III: Response protocol to the host

The microcontroller status is sent to the host only when a Slave Response Header frame is received. The microcontroller status is always sent in a transfer block of 9 Bytes.

A typical transfer block consists of four parts:

NAD (1 byte)	Response (1 byte)	Response Data (6 bytes)	Checksum (1 byte)

- **NAD**: Node Address for Diagnostic, specifies the address of the active slave node.
- **Response**: Response code indicating Acknowledge or Error status. See **Table 4-7**.
- **Response Data**: These 6 Bytes are generally not used and set to 00_H. An exception is mode A response which is described in detail in **Section 4.5.3**.
- **Checksum**: The checksum is calculated based on NAD, Response and Response Data Bytes. All responses sent by microcontroller will adopt classic checksum. See **Section 4.4.3.1**.

4.5.1 Acknowledgement response

The Acknowledge response code (55_H) is sent by microcontroller to host to indicate that a block has been successfully received.

4.5.2 Error response

There are 3 error responses indicated by microcontroller.

4.5.2.1 Block Type Error (FF_H)

This error can occur in the following conditions.

1. A Block Type other than the implemented ones was received. See **Table 4-2**.
2. An incorrect sequence of transfer blocks was received. For example, in mode 0 operation upon receiving a header block, a slave response request is expected. However, if another header block is received, this will result in a Block Type Error.

4.5.2.2 Checksum Error (FE_H)

This error occurs when the checksum comparison fails. Microcontroller will reject the transfer block by sending back a Checksum Error code (FE_H) to the host.

4.5.2.3 Protection Error (FD_H)

This error occurs when selected NVM sectors, for programming or erasing, are protected. As the selected NVM sectors are protected, no programming or erasing is allowed. In this special error case, the LIN routine will abort current command and wait for the next header block from the host again.

4.5.2.4 Response overview

Table 4-5 shows a tabulated summary of the possible responses the device may transmit following the reception of a header, data or EOT block.

Table 4-5 Possible responses for various block types

Mode	Header block	Data block	EOT block
0, 2, 8	Acknowledge, Block Type Error, Checksum Error, Protection Error	Acknowledge, Block Type Error, Checksum Error	Acknowledge, Block Type Error, Checksum Error
1, 3, 9	Acknowledge, Block Type Error, Checksum Error		
4, 6	Acknowledge, Block Type Error, Checksum Error, Protection Error		
A	Acknowledge, Block Type Error, Checksum Error		

The responses are defined in Table 4-6, which lists the possible reasons and/or implications for error and suggests the possible corrective actions that the host can take upon notification of the error.

Table 4-6 Definitions of responses

Response	Value	Description			
		Block Type	BSL Mode	Reasons / Implications	Corrective Action
Acknow-ledge	55_H	Header	1, 3, 9	The requested operation will be performed once the response is sent.	
			A	The requested operation has been performed and is successful. 4 Byte data transmission follows.	
			6	The requested operation has been performed and is successful.	
		EOT	0, 2, 4, 8		
		All other combinations		Reception of the Block is successful. Ready to receive the next block.	

Table 4-6 Definitions of responses (cont'd)

Response	Value	Description			
		Block Type	BSL Mode	Reasons / Implications	Corrective Action
Block Type Error	FF_H	Header	2, 4	NVM start address out of range.	Retransmit a valid header block.
		All other combinations		Either the block Type is undefined or the flow is invalid (see Figure 4-2).	Retransmit a valid block
Checksum Error	FE_H	All combinations		There is a mismatch between the calculated and the received Checksum (see Section 4.4.3).	Retransmit the block
Protection Error	FD_H	Header	0, 2, 4, 6, 8	Protection against external access enabled, i.e. NVM_PASSWORD is valid.	Disable protection
	FD_H	Header	6	User-password invalid (set either to 00_H or FF_H) on an unprotected device.	Repeat command with valid password

Table 4-7 gives a summary of the response codes to be sent back to the host by the microcontroller.

Table 4-7 Type of Response Code

Communication status	Response code to the host
Acknowledge (Success)	55_H
Block Type Error	FF_H
Checksum Error	FE_H
Protection Error	FD_H

4.5.3 Mode A response

This response frame is only applicable for mode A. The response frame depends on the option Byte value used.

Option Byte = 00_H:

NAD (1 byte)	ACK Response 55_H	ID (1 bytes)	CHIP_ID_2 (1 bytes)	CHIP_ID_1 (1 bytes)	CHIP_ID_0 (1 bytes)	Not Used (2 bytes)	Checksum (1 byte)

Refer to **Chapter 6.2.1** for Chip_ID definition.

Option Byte = 10_H, 18_H, 50_H:

NAD (1 byte)	ACK Response 55_H	Error indicator (1 bytes)	Calculated CHKS High (1 bytes)	Calculated CHKS Low (1 bytes)	Not Used (3 bytes)	Checksum (1 byte)

Error indicator:

- 00_H: the calculated checksum and the expected one (provided as an input in the header frame) are equal.
- 80_H: the calculated checksum and the expected one (provided as an input in the header frame) differ.

4.6 Fast LIN BSL

Fast LIN BSL is an enhanced feature in TLE986xQX device, supporting higher baud rates up to 57.6 kBaud or 115.2 kBaud. To support this faster baudrate, once entered to Fast LIN BSL, the protocol used will be the same as UART BSL (refer to **Chapter 5** for transfer protocol).

This mode is especially useful during back-end programming, where faster programming time is desirable.The Fast LIN BSL is not meant to be used for in-car communication since it is not protected against noise on the LIN line.

4.6.1 Entering Fast LIN BSL

User can enter Fast LIN BSL using an invalid NAC, using a dedicated NAC value (refer to **Table 3-1**) or by sending a LIN command frame with Fast_Prog set to 1. (See **Section 4.4.4.2**, the Fast_Prog option Byte is supported in LIN BSL modes 0, 2 and 8).

Note: LIN BSL will no longer be supported in future revisions of this product. All the LIN BSL features will be supported by FastLIN BSL but with higher baudrate. Access to Fast LIN BSL will then be ensured only via proper NAC setting.

In case the Fast LIN is entered via LIN command frame by setting the Fast_Prog option, all other information sent with the frame are ignored. The baud rate, used for the Fast

LIN BSL, is calculated based on the Master Request Header + Command LIN frame received. The LIN transceiver slope mode is set to Flash mode, a specific setting of the internal slew rate control that allows transmission up to 115.2 kBaud, and set the baudrate according to the received LIN frame. The Fast LIN BSL entry is shown in **Figure 4-5**.

In case, instead, the Fast LIN is entered directly via proper or invalid NAC, the protocol is soon changed to UART. In this last case, the device still expects to receive a UART test byte (80_H) but the baudrate is not calculated based on the received test byte and is instead by default set to 115.2 kBaud after having properly set the transceiver slope mode to Flash mode.

The LIN transceiver slope mode is set back to normal mode before jumping to user code via mode 1 or mode 3.

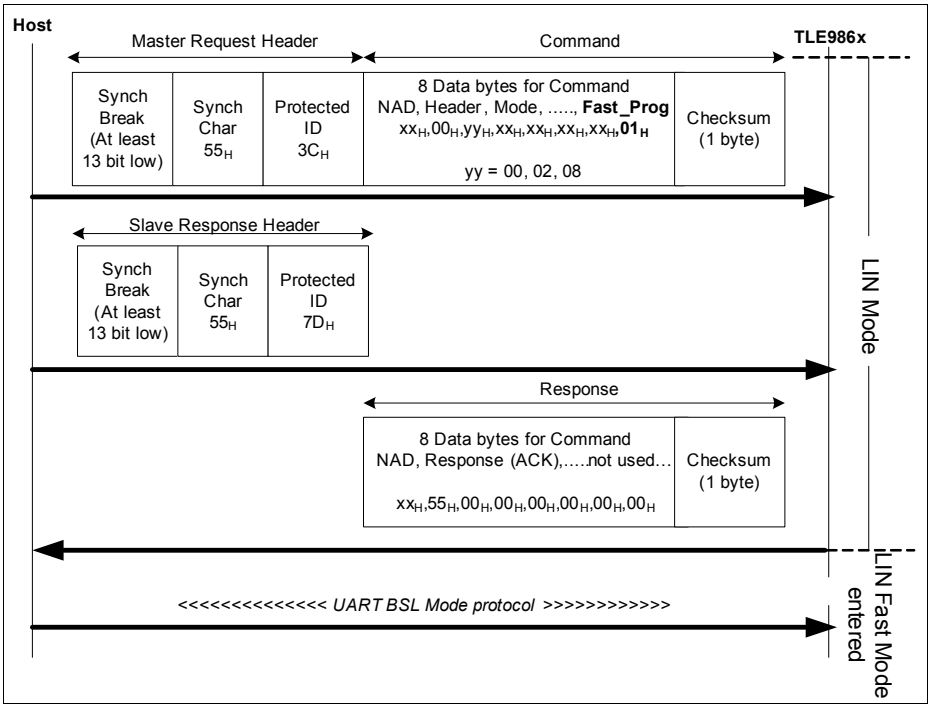

Figure 4-5 Fast LIN BSL mode entry

4.7 After-Reset conditions

When more than one parameter in the transfer block is invalid, different actions are performed. The different scenarios, and its consequent actions, are listed in **Table 4-8**.

Table 4-8 LIN BSL After-Reset conditions

First Frame	ID	Check sum	NAD	Block Type (Header only)	Mode	Action
Yes	Invalid	Don't care	Don't care	Don't care	Don't care	Save LIN Message to RAM[1] and jump to NVM 11000004_H[2)3)].
No	Invalid	Don't care	Don't care	Don't care	Don't care	Message is ignored. Wait for next frame.
Yes	$7D_H$	N.A.	N.A.	N.A.	N.A.	Save LIN ID to RAM[1] and jump to NVM 11000004_H[2)3)]
No	$7D_H$	N.A.	N.A.	N.A.	N.A.	Reply if there is a previous valid Master Request (Command Frame) else wait for next frame
Yes	$3C_H$	LIN	Don't care	Invalid	Valid[4)]	Error flag is triggered. Wait for Response frame to reflect error
Yes	$3C_H$	LIN	Don't care	Don't care	Invalid[4)]	Save LIN message to RAM[1] and jump to NVM 11000004_H[2)3)]
Yes	$3C_H$	LIN	Valid	Valid	Valid[4)]	Execute command
Yes	$3C_H$	LIN	Invalid	Valid	Valid[4)]	Message is ignored. Wait for next frame.
Yes	$3C_H$	Prog	Invalid	Don't care	Don't care	Message is ignored. Wait for next frame.
Yes	$3C_H$	Prog	Valid	Invalid	Valid[5)]	Error flag is triggered. Wait for Response frame to reflect error
Yes	$3C_H$	Prog	Valid	Valid	Invalid[5)]	Error flag is triggered. Wait for Response frame to reflect error
Yes	$3C_H$	Prog	Valid	Valid	Valid[5)]	Execute command
Yes	$3C_H$	Invalid	Don't care	Don't care	Don't care	Save LIN message to RAM[1] and jump to NVM 11000004_H[2)3)]

1) The LIN frame will be saved and dumped for debugging at RAM address 18000500H.

2) Jump to user mode will only occur either (1) when NVM is not protected and NVM content at 11000004_H is not FF_H or (2) when NVM is protected.

3) Up to max 10 Bytes are saved into the RAM. In case less than 10 Bytes are received, firmware proceeds to user code after a time out of 35 ms.

4) Valid modes for LIN checksum are mode 8 and mode 9. Other modes are considered invalid.

5) Valid modes for programming checksum are mode 0-6 and A. Other modes are considered invalid.

4.8 BSL Mode User Parameters – NAC/NAD

There are 2 programmable parameters in the uppermost linearly mapped NVM Bank that are used in LIN BSL. The parameter values are specified by the user:

1. No Activity Count (NAC): Defines the duration of BSL connection acceptance window (in multiple of 5ms) starting from the reset release.
2. Node Address for Diagnostic (NAD): Specifies the node address used for the LIN BSL communication.

Note: Timer 21 is initialized to have 5 ms overflow and is used to create the delay.

The BootROM will detect any activities on the LIN bus for a period of time, determined by (((NAC & $3F_H$) -01_H) * 5) ms. When nothing is detected on the LIN bus during this time, it will jump to user mode.

Note: For FastLIN protocol any pulse on the LIN bus causes entering BSL mode. The NAC counter will be stopped. The BootROM will even then stay in BSL mode if no valid BSL command is received at all. This means, unexpected noise on the LIN bus might cause unwanted entering of the BSL mode and therefore might prevent normal user code execution. In order to overcome this behavior the BootROM internal BSL mode shall be disabled by the user application by setting the NAC value to X1h or by selecting LIN BSL protocol.

NAC value is restricted to $0C_H$ as the first open WDT1 window is worst case 65 ms. The firmware has to either refresh the WDT within the 65 ms or jump to user mode. If NAC value is bigger than $0C_H$, BootROM code will refresh the WDT and wait for a LIN frame indefinitely.

4.8.1 Programming NAC and NAD

User needs to program the NAC and NAD in the format listed in **Table 3-3**. To ensure the parameter validity, the 2 parameters actual values and their inverted values are checked.

If the NAD parameter is not valid nor within the range, the default value ($7F_H$) is used in the LIN BSL.

4.9 WDT1 refreshing

After a reset the WDT1 is starting with a long open window. WDT1 keeps on running while waiting for first LIN frame. In case during the LIN BSL waiting time, defined by NAC, a LIN communication is detected, WTD1 is disabled and its status frozen.

Subsequently, before exiting to RAM or NVM in LIN BSL modes 1, 3 and 9 the watchdog is re-enabled and starts from the previously frozen state. The WDT1 is then still in long open window and the remaining valid time is equal to Long open window minus the time between reset release and first LIN communication. User program needs to trigger the WDT1 refresh accordingly.

5 FastLIN BSL Mode (UART BSL)

This chapter describes the protocol used for the FAST LIN and UART BSL.

The protocol is based on the phases described following.

- **Phase I**: Establish a serial connection and automatically synchronize to the transfer speed (baud rate) of the serial communication partner (host).
- **Phase II**: Perform the serial communication with the host. The host controls the communication by sending special header information which selects one of the working modes. These modes are:
  - **Mode 0 (00_H)**: Transfer a user program from the host to RAM or write 100TP pages[1)]
  - **Mode 1 (01_H)**: Execute a user program in the RAM[2)]
  - **Mode 2 (02_H)**: Transfer a user program from the host to NVM[1)]
  - **Mode 3 (03_H)**: Execute a user program in the NVM[2)]
  - **Mode 4 (04_H)**: Erase NVM[1)]
  - **Mode 6 (06_H)**: NVM protection mode enabling/disabling Scheme[2)]
  - **Mode A ($0A_H$)**: Get Info (based on Option Byte)[1)]

Except mode 1, mode 3 and mode 6, the microcontroller would return to the beginning of Phase II and wait for the next command from the host after executing all other modes.

The serial communication, which is activated in Phase II, is performed via the integrated LIN transceiver for FastLIN and via with the full-duplex serial interface (UART) of the TLE986xQX for UART BSL.

The serial transfer is working in asynchronous mode with the serial parameters 8N1 (eight data Bits, no parity and one stop Bit). The host can vary the baud rate in a wide range because the microcontroller does an automatic synchronization to the host in Phase I.

The following section provides detailed information on these two UART BSL phases.

5.1 Phase I: Automatic serial synchronization to the host

Upon entering UART BSL mode, a serial connection is established and the transfer speed (baud rate) of the serial communication partner (host) is automatically synchronized in the following steps:

- STEP 1: Initialize serial interface for reception and timer for baud rate measurement
- STEP 2: Wait for test Byte (80_H) from host
- STEP 3: Synchronize the baud rate to the host
- STEP 4: Send Acknowledge Byte (55_H) to the host
- STEP 5: Enter Phase II

1) The microcontroller returns to the beginning of phase II and waits for the next command from the host
2) UART BSL and serial communication are terminated.

5.1.1 General description

The microcontroller will set the serial port to mode 1 (8-bit UART, variable baud rate) for communication. Timer 2 will be set in auto-reload mode (16-bit timer) for baud rate measurement. In the process of waiting for the test Byte (80_H), microcontroller will start the timer on reception of the start Bit (0) and stop it on reception of the last Bit of the test Byte (1). Then the UART BSL routine calculates the actual baud rate, sets the PRE and BR_VALUE values and activates baud rate generator. When the synchronization is done, the microcontroller sends back the Acknowledge Byte (55_H) to the host. If the synchronization fails, the baud rates for the microcontroller and the host are different, and the Acknowledge code from the microcontroller cannot be received properly by the host. In this case, on the host side, the host software may give a message to the user, e.g. asking the user to repeat the synchronization procedure. On the microcontroller side, the UART BSL routine cannot judge whether the synchronization is correct or not. It always enters phase II after sending the Acknowledge Byte. Therefore, if synchronization fails, a reset of the microcontroller has to be invoked, to restart it for a new synchronization attempt.

5.1.2 Calculation of BR_VALUE and PRE values

For the baud rate synchronization of the microcontroller to the fixed baud rate of the host, the UART BSL routine waits for a test Byte (80_H), which has to be sent by the host. By polling the receive port of the serial interface (P1_DATA.4/RxD Pin), the Timer 2 is started on the reception of the start Bit (0) and stopped on the reception of the last Bit of the test Byte (1). Hence the time recorded is the receiving time of 8 Bits (1 start Bit plus 7 least significant Bits of the test Byte). The resulting timer value is 16-bit (T2). This value is used to calculate the 11-bit auto-reload value (BR_VALUE stored in the BGH and BGL SFRs), the fractional divider FDSEL and PRE, with T2PRE predefined as 011. This calculation needs two formulas.

First, the correlation between the baud rate (baud) and the reload value (BG) depends on the internal peripheral frequency (f_{PCLK})

$$\text{baud} = \frac{f_{PCLK}}{16 \times PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right)} \quad [5.1]$$

Second, the relation between the baud rate (baud) and the recording value of Timer 2 (T2) depends on the T2 peripheral frequency (f_{T2}) and the number of received Bits ($f_{T2}N_b$)

$$\text{baud} = \frac{f_{T2} \times N_b}{T2} \quad [5.2]$$

Combining **Equation [5.1]** and **Equation [5.2]** with N_b=8, f_{T2}=f_{PCLK}/ 8 (T2PRE=011),

$$\frac{f_{PCLK}}{16 \times PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right)} = \frac{\frac{f_{PCLK}}{8} \times 8}{T2} \quad [5.3]$$

Simplifying **Equation [5.3]**, we get

$$PRE \times \left(BR\_VALUE + \frac{FDSEL}{32}\right) = \frac{T2}{16} \quad [5.4]$$

After setting BR_VALUE, FDSEL and PRE, the baud rate generator will then be enabled, and the UART BSL routine sends an Acknowledge Byte (55_H) to the host. If this Byte is received correctly, it will be guaranteed that both serial interfaces are working with the same baud rate.

5.2 Phase II: Serial communication protocol and the working modes

After the successful synchronization to the host, the UART BSL routine enters Phase II, during which it communicates with the host to select the desired working modes. The detailed communication protocol is explained as follows:

5.2.1 Serial communication protocol

The communication between the host and the UART BSL routine is done by a simple transfer protocol. The information is sent from the host to the microcontroller in blocks. All the blocks follow the specified block structure. The host is sending several transfer blocks and the UART BSL routine is just confirming them by sending back single Acknowledge or error Bytes. The microcontroller itself does not send any transfer blocks.

However, the above regulation does not apply to some modes where the microcontroller might need to send the required data to the host besides the Acknowledge or error Byte (e.g. mode A).

5.2.1.1 Transfer block structure

A transfer block consists of three parts:

Block Type (1 byte)	Data Area (X bytes)	Checksum (1 byte)

- **Block Type**: the type of block, which determines how the Bytes in the data area are interpreted. Implemented block types are:
  - 00_H type “Header”
  - 01_H type “Data”
  - 02_H type “End of Transmission” (EOT)
- **Data area**: A list of Bytes, which represents the data of the block. The length of data area cannot exceed 128 Bytes for mode 0 and 2. For mode 2, the length of data area must always be 128 Bytes. This is due to the fact that NVM is written page-wise.
- **Checksum**: the XOR checksum of the Block Type and data area.

The host will decide the number of transfer blocks and their respective lengths during one serial communication process. For safety purpose, the last Byte of each transfer block is a simple checksum of the Block Type and data area. The host generates the checksum by XOR-ing all the Bytes of the Block Type and data area. Every time the UART BSL routine receives a transfer block, it recalculates the checksum of the received Bytes (Block Type and data area) and compares it with the attached checksum.

Note: If there is less than one page to be programmed to NVM, the PC host will have to fill up the vacancies with 00_H, and transfer data in the length of 128 Bytes.

5.2.1.2 Transfer block type

There are three types of transfer blocks depending on the value of the Block Type. **Table 5-1** provides the general information on these block types. More details will be described in the corresponding sections later.

Table 5-1 Type of transfer block

Block Name	Block Type	Description
Header block	00_H	This block has a fixed length of 8 Bytes. Special information is contained in the data area of the block, which is used to select different working modes.
Data block	01_H	This block length depends on the special information given in the previous header block. This block is used in working mode 0 and 2 to transfer a portion of program code. The program code is contained in the data area of the block.
EOT block	02_H	This block length depends on the special information given in the previous header block. This block is the last block in data transmission in working mode 0 and 2. The last program code to be transferred is in the data area of the block.

5.2.1.3 Response codes to the host

The microcontroller communicates to the host whether a block has been successfully received by sending out a response code. If a block is received correctly, an Acknowledge Code (55_H) is sent. In case of failure, an error code is returned. There are two possible error codes, FF_H or FE_H, reflecting the two possible types of fail, Block Type or Checksum Error. A Block Type Error occurs when either a not implemented Block Type or transfer blocks in wrong sequence are received. For example, if in working mode 0 two consecutive header blocks are received a Block Type Error is detected and a Block Type Error (FF_H) indication is returned. A Checksum Error occurs when the checksum comparison on a received block fails. In such a case, the transfer is rejected and a Checksum Error (FE_H) indication is returned. In both error cases the UART BSL routine awaits the actual block from the host again.

When program and erase operation of NVM is restricted due to enabled NVM protection, only modes 1, 3 and some options of mode A are allowed. All other modes are blocked and a Protection Error code (FD_H) will be sent to host. This will indicate that NVM is protected and no programming and erasing are allowed. In this error case, the UART BSL routine will wait for the next header block from the host again.

Table 5-2 gives a summary of the response codes to be sent back to the host by the microcontroller after it receives a transfer block.

Table 5-2 Type of response codes

Communication status	Response code to the host
Acknowledge (Success)	55_H
Block Type Error	FF_H
Checksum Error	FE_H
Protection Error	FD_H
Combined Offset Error (COMBOFFSETFAULT)	$0FB_H$ only valid for Mode 0 option $F0_H$
ID Offset Error (IDOFFSETFAULT)	$0FA_H$ only valid for Mode 0 option $F0_H$
In Page Offset Error (INPAGEOFFSETFAULT)	$0F9_H$ only valid for Mode 0 option $F0_H$

Table 5-3 shows a tabulated summary of the possible responses the device may transmit following the reception of a header, data or EOT block.

Table 5-3 Possible responses for various block types

Mode	Header block	Data block	EOT block
0	Acknowledge, Block Type Error, Checksum Error, Protection Error	Acknowledge, Block Type Error, Checksum Error	Acknowledge, Block Type Error, Checksum Error, Combined/ID/InPage offset error
1	Acknowledge, Block Type Error, Checksum Error		
2	Acknowledge, Block Type Error, Checksum Error, Protection Error	Acknowledge, Block Type Error, Checksum Error	Acknowledge, Block Type Error, Checksum Error
3	Acknowledge, Block Type Error, Checksum Error		
4	Acknowledge, Block Type Error, Checksum Error, Protection Error		

Table 5-3 Possible responses for various block types (cont'd)

Mode	Header block	Data block	EOT block
6	Acknowledge, Block Type Error, Checksum Error, Protection Error		
A	Acknowledge, Block Type Error, Checksum Error, Protection Error		

The responses are defined in **Table 5-4**, which lists the possible reasons and/or implications for error and suggests the possible corrective actions that the host can take upon notification of the error.

Table 5-4 Definitions of responses

Response	Value	Description			
		Block Type	BSL Mode	Reasons / Implications	Corrective Action
Acknow-ledge	55_H	Header	1, 3	The requested operation will be performed once the response is sent.	
			A	The requested operation has been performed and was successful. Requested data transmission follows.	
			6	The requested operation has been performed and was successful.	
		EOT	0, 2, 4		
		All other combinations		Reception of the block was successful. Ready to receive the next block.	
Block Type Error	FF_H	Header	2, 4, A	Start Address in Mode Data is not within NVM address range or invalid CS Page.	Retransmit a valid header block.
		All other combinations		Either the Block Type is undefined or option is invalid or the flow is invalid.	Retransmit a valid block
Checksum Error	FE_H	All combinations		There is a mismatch between the calculated and the received Checksum.	Retransmit a valid block

Table 5-4 Definitions of responses (cont'd)

Response	Value	Description			
		Block Type	BSL Mode	Reasons / Implications	Corrective Action
Protection Error	FD_H	Header	0, 2, 4, 6, A	Protection against external access enabled, i.e. user-password is valid.	Disable protection
Combined Offset Error Code	FB_H	EOT	0	The operation is targeting 100-TP page 1 and there is at least 1 Byte with a not in page offset and 1 byte pointing to the Customer_ID reserved region.	Check the Byte offset.
ID Offset Error Code	FA_H	EOT	0	The operation is targeting 100-TP page 1 and there is at least 1 Byte pointing to the Customer_ID reserved region.	Check the Byte offset.
Combined Offset Error Code	$F9_H$	EOT	0	There is at least 1 Byte with a not in page offset.	Check the Byte offset.

5.2.1.4 Block response delay

As described in **Section 5.2.1.3**, after receiving any block the microcontroller communicates to the host whether the block was successfully received by sending out a response code. If a block is received correctly, an Acknowledge Code (55H) is sent. In case of failure, an error code is returned.

The response is transmitted with a delay that depends on the selected mode and on the type of the block received.

The following **Table 5-5** reports the maximum response delay for each mode and block type.

Table 5-5 Maximum Response Delay

Max Response Delay Table					
			Block Type		
Mode	Option	Description	Header	Data	EoT
Mode 0	0x00	Download Code/ Data to RAM	250 us	1 µs per Byte	1 µs per Byte
	0xF0	Download data to 100TP pages	250 µs	1 µs per Byte	10 ms [1]
Mode 1	--	RAM code execution	250 µs	--	--
Mode 2	--	Download Code/ Data to NVM	250 µs	10 ms [1]	10 ms [1]
Mode 3	--	NVM code execution	250 µs	--	--
Mode 4	0x00	NVM page erase	4.5 ms	--	--
	0x40	NVM sector erase	4.5 ms	--	--
	0xC0	NVM mass erase	4.5 ms per sector	--	--
Mode 6	--	NVM Protection set	10 ms [1]	--	--
	--	NVM Protection reset	4.5 ms + 4.5 ms per sector	--	--
Mode A	0x00	Get Chip ID	250 µs	--	--
	0x10	NVM Page Checksum Check	250 µs	--	--
	0x18	NVM Mass checksum check	100 ms	--	--
	0x50	100TP page Checksum Check	250 µs	--	--
	0xC0	NVM Page	250 µs	--	--
	0xF0	100TP page	250 µs	--	--

[1] Time needed for data collection, OpenAB, erasing old data (if required) and programming the data given

5.2.2 UART BSL Modes

When the UART BSL routine enters Phase II, it first waits for an 8-byte long header block from the host. The header block contains the information for the selection of the working modes. Depending on this information, the UART BSL routine selects and activates the desired working mode. If the microcontroller receives an incorrect header block, the UART BSL routine sends, instead of an Acknowledge code, a Checksum or Block Type Error code to the host and awaits the header block again. In this case the host may react by re-sending the header block or by releasing a message to the user.

5.2.2.1 Header Block

The header block is always the first transfer block to be sent by the host during one data communication process. It contains the working mode number and special information on the related mode (referred to as “Mode Data”). The general structure of a header block is shown below.

Block Type $\mathbf{00_H}$ (Header Block)	**Data Area**		**Checksum** (1 byte)
	Mode (1 byte)	**Mode Data** (5 bytes)	

Description:

- **Block Type** $\mathbf{00_H}$: The Block Type, which marks the block as a **header block**
- **Mode**: The mode to be selected. The implemented modes are covered in **Section 5**
- **Mode Data**: Five Bytes of special information, which are necessary to activate corresponding working mode.
- **Checksum**: The checksum of the header block.

5.2.2.2 Mode 0 - Code/Data download to RAM/100TP

Mode 0 is used to transfer a user program or data from the host to the RAM of the microcontroller via serial interface. Selecting the proper mode option, this mode can be used to transfer data into the user configuration sector pages. In this case, user has to transfer data to the RAM in accordance with the format reported in the **Table 6-12** and after EOT block has been received, data is automatically copied with proper offset in the target page. If NVM protection is installed, programming to RAM is not allowed.

Different options supported are:

- Option 00_H: RAM download
- Option $F0_H$: RAM download and Configuration sector page programming

The header block for this working mode has the following structure:

The header block for RAM download (Option = 00_H)

00_H (Header Block)	00_H (Mode 0)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr High (1 byte)	StartAddr Low (1 byte)	Block Length (1 byte)	Not Used (1 byte)	Option = 00_H (1 byte)	

Mode Data Description:

Start Addr High, Low: 16-bit Start Address, which determines where to copy the received program codes into the RAM.

Block Length: The length (number of Bytes) of the following data blocks or EOT block.

Not Used: this Byte is not used and will be ignored.

Option: Set to 00_H for RAM download.

Note: RAM Address provided as input in mode 0 has to be considered as an offset to be added to the standard RAM starting address of the TLE986xQX.

In option 00H start address can be each valid RAM offset address. Data sent in the following data/ EOT blocks will be copied into the RAM at the specified address (18000000_H + StartAddr).

The header block for RAM download and CS page programming (Option = $F0_H$)

00_H (Header Block)	00_H (Mode 0)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr High (1 byte)	StartAddr Low (1 byte)	Block Length (1 byte)	CS Page (1 byte)	Option = $F0_H$ (1 byte)	

Mode Data Description:

Start Addr High, Low: 16-bit Start Address, which determines where to copy the received data in the RAM.

Block Length: The length of the following data blocks or EOT block.

CS Page: This Byte is used to select the desired user configuration sector page to be programmed. This Byte is relevant only in case option $F0_H$ is used. CS page is selected according to the addressing scheme reported in **Figure 6-2**.

Option: Set to $F0_H$ for RAM download and CS page programming

Using this option, user can write data into the user CS pages (100TP pages). In this case, data has to be sent to the RAM according to the **Table 6-12** and therefore start address has to be equal to 18000400_H. In case a different starting address is provided, the operation will result in a Block Type Error indication. When this option is selected a proper CS page has to be provided.

Note: RAM Address provided as input in mode 0 has to be considered as an offset to be added to the standard RAM starting address of the TLE986xQX. *So, for option* $F0_H$, the Start Addr parameter has to be set to 0400_H.

All other options will be treated as option 00_H.

*Note: The **Block Length** refers to the whole length (Block Type, data area and checksum) of the following transfer block (data block or EOT block).*

After successfully receiving the header block, the microcontroller enters mode 0, during which the program codes are transmitted from the host to the microcontroller by data block and EOT block, which are described as below.

The data block

01_H (Data Block)	**Program Code** (((Block Length) - 2) bytes)	**Checksum** (1 byte)

Description:

Program Code: The program code has a length of ((**Block Length**) - 2) Byte, where the **Block Length** is provided in the previous header block.

The EOT block

02_H (EOT Block)	**Last Codelength** (1 byte)	**Program Code** (Last Codelength bytes)	**Not Used** (((Block Length) – 3 – (Last Codelength)) bytes)	**Checksum** (1 byte)

Description:

Last Codelength: This Byte indicates the length of the program code in this EOT block.

Program Code: The last program code to be sent to the microcontroller

Not used: The length is ((**Block Length**) - 3 - (**Last Codelength**)) Bytes.

When trying to program config sector, some special error handling is provided.

In particular, in addition to the generic error code, the UART BSL Mode 0 option $F0_H$ may return:

- BLOCKFAULT indication (FF_H) in case of wrong config sector page selection
- INPAGEOFFSETFAULT indication ($F9_H$) in case at least one byte has an offset > $7E_H$, i.e. has a not in page offset or is targeting the page counter (refer to **Table 6-12**). In this case, the program for the valid Bytes is still performed.
- IDOFFSETFAULT indication (FA_H) in case at least one byte is targeting the Customer_ID reserved region when programming 100TP page 1. In this case, the program for the valid Bytes is still performed.
- COMBOFFSETFAULT indication (FB_H) in case at least one byte is targeting the Customer_ID reserved region when programming 100TP page 1 and at least 1 Byte has a not in page offset or is targeting the page counter. In this case, the program for the valid Bytes is still performed.

5.2.2.3 Mode 1 - Code Execution inside RAM

Mode 1 is used to execute a user program in the RAM of the microcontroller at the address pointed by the RAM location 18000404_H. The header block for this working mode has the following structure:

The header block

00_H (Header Block)	**01_H** (Mode 1)	**Mode Data (5 bytes)**	**Checksum** (1 byte)
		Not Used	

Mode Data Description:

Not used: The five Bytes are not used and will be ignored in mode 1.

In working mode 1, the header block is the only transfer block to be sent by the host, no further serial communication is necessary. The microcontroller will exit the UART BSL mode, set the vector table in RAM at address 18000400_H and branch to the address pointed by the standard reset handler (18000404_H).

5.2.2.4 Mode 2 - Code/Data download to NVM

Mode 2 is used to transfer a user program from the host to the NVM of the microcontroller via serial interface. This mode is not accessible if NVM protection is installed.

The header block for this working mode has the following structure:

The header block

00_H (Header Block)	02_H (Mode 2)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr 4 (MSB)	StartAddr 3	StartAddr 2	StartAddr 1 (LSB)	Block Length (1 byte)	

Mode Data Description:

Start Addr 4, 3, 2, and 1: 32-bit Start Address, which determines where to copy the received program codes in the NVM. This address must be aligned to the page address.

Block Length: The length of the following data blocks or EOT block. If data blocks are to be sent, the block length has to be 130 (128+2) Bytes. If only EOT block is sent, the block length has to be 131 (128+3) Bytes. Other block length values than 130 (data block) or 131 (EOT block) are not allowed.

*Note: If the data starts in a non-page address, PC host must fill up the beginning vacancies with 00_H and provide the start address of that page. For e.g., if data starts in $11000F82_H$, the PC host will fill up the addresses $11000F80_H$ and $11000F81_H$ with 00_H and provide the **Start Address** $11000F80_H$ to microcontroller. Moreover, if data is only 8 Bytes, the PC host will also fill up the remaining addresses with 00_H and transfer 128 data Bytes.The **Block Length** refers to the whole length (Block Type, data area and Checksum) of the following transfer block (data block or EOT block).*

After successfully receiving the header block, the microcontroller enters mode 2, during which the program codes are transmitted from the host to the microcontroller by data block and EOT block, which are described as below.

The data block

01_H (Data Block)	Program Codes (((Block Length) - 2) bytes)	Checksum (1 byte)

Description:

Program Codes: The program codes have a length of ((**Block Length**) - 2) Bytes, where **Block Length** is provided in the previous header block.

The EOT block

02_H (EOT Block)	**Last Codelength** (1 byte)	**Program Code** (Last Codelength bytes)	**Not Used** (((Block Length) – 3 – (Last Codelength)) bytes)	**Checksum** (1 byte)

Description:

Last Codelength: This Byte indicates the number of program code bytes in this EOT block.

Program Code: The last program code bytes to be sent to the microcontroller

Not used: The length is ((**Block Length**) - 3 - (**Last Codelength**)) Bytes.

The following Figures show examples of how to program one or several NVM pages using working mode 2.

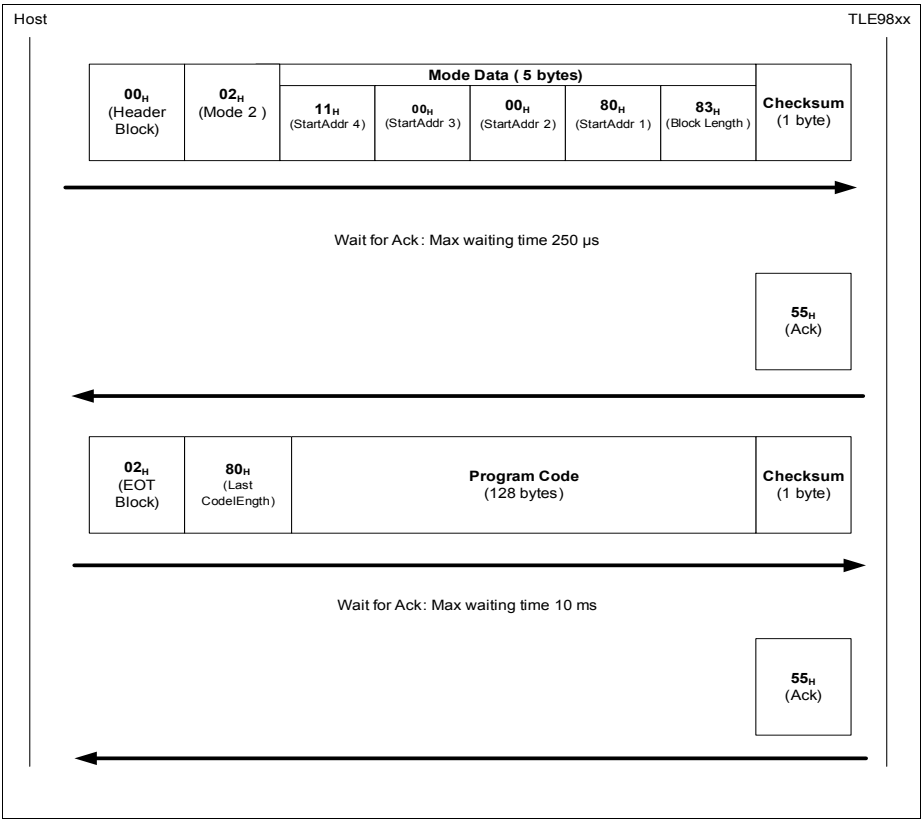

Figure 5-1 Single NVM Page program via working mode 2

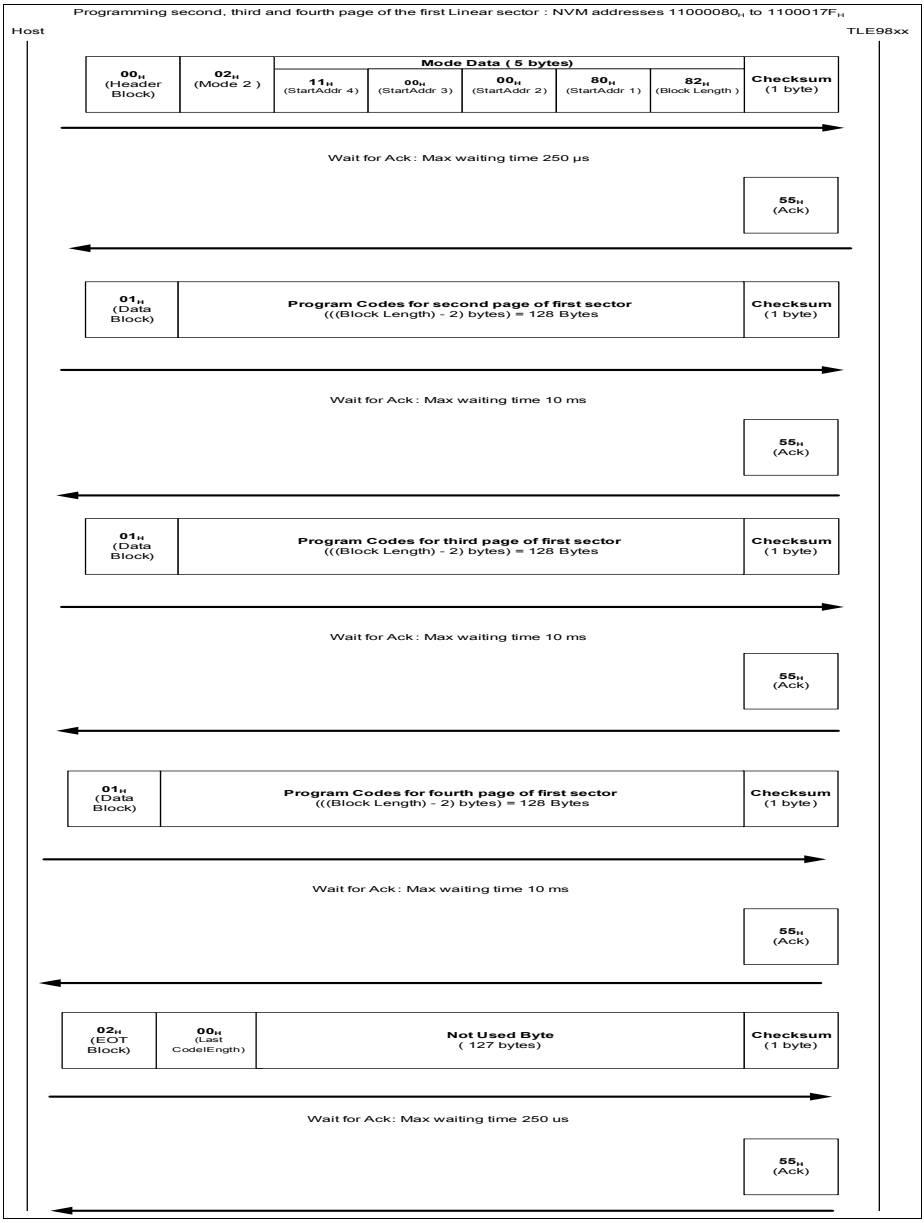

Figure 5-2 Multiple NVM Page program via working mode 2

5.2.2.5 Mode 3 - Code Execution inside NVM

Mode 3 is used to execute a user program in the NVM of the microcontroller at the address pointed by the NVM location 11000004_H. The header block for this working mode has the following structure:

The header block

00_H (Header Block)	**03_H** (Mode 3)	**Mode Data (5 bytes)**	**Checksum** (1 byte)
		Not Used	

Mode Data Description:

Not used: The five Bytes are not used and will be ignored in mode 3.

In working mode 3, the header block is the only transfer block to be sent by the host, no further serial communication is necessary. The microcontroller will exit the UART BSL mode, set the vector table in NVM at the address 11000000_H and jump to the address pointed by the NVM location 11000004_H.

Note: Jump to NVM will only occur when either (1) NVM is not protected and NVM content at 11000004_H is not FF_H or (2) when NVM is protected. In all other cases, firmware will put the device in sleep mode.

5.2.2.6 Mode 4 - NVM Erase

Mode 4 is used to erase different areas of the NVM. It supports mass erase of all the NVM sectors, individual erase of the sectors for linear area or for non-linear area and single page erase. This is determined by the Option Byte. This mode is not accessible if the NVM protection is enabled.

Different options supported are:

- Option 00_H : NVM page erase
- Option 40_H : NVM sector erase
- Option $C0_H$: NVM Mass erase

The header block for NVM page erase (with Option = 00_H)

00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr 4 (MSB)	**StartAddr 3**	**StartAddr 2**	**StartAddr 1** (LSB	**Option =00_H** (1 byte)	

Mode Data Description:

Start Addr High, Low: 32-bit Start Address, which determines which NVM page to be erased. Address should be page aligned.

Option: Set to 00_H for page erase

When the Option Byte = 00_H, this mode performs an erase of the NVM page specified by the provided address.

The header block for NVM sector erase: (with Option = 40_H)

00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr 4 (MSB)	**StartAddr 3**	**StartAddr 2**	**StartAddr 1** (LSB	**Option = 40_H** (1 byte)	

Mode Data Description:

Start Addr High, Low: 32-bit Start Address, which determines which NVM sector to be erased. Address should be sector aligned.

Option: Set to 40_H for sector erase

When the Option Byte = 40_H, this mode performs an erase of the NVM sector specified by the provided address. The time taken to erase a sector is max 4.5 ms.

The header block for NVM mass erase: (with Option = $C0_H$)

00_H (Header Block)	04_H (Mode 4)	Mode Data (5 bytes)		Checksum (1 byte)
		Not Used (4 bytes)	**Option =$C0_H$** (1 byte)	

Mode Data Description:

Not used: The four Bytes are not used and will be ignored in option $C0_H$.

Option: Set to $C0_H$ for mass erase

When the Option Byte = $C0_H$, this mode performs a mass erase of all the NVM sectors. The time taken will be max. 4.5 ms * number of sectors, as the erase operation is done sequentially.

Note:

1. *In mode 4, a Block Type Error will be sent, if an invalid option Byte is received. Once password is set, no access to mode 4 is allowed and Protection Error will be sent.*
2. *NAC and NAD values will also be erased and the device will no longer be accessible in UART BSL, because NAC is invalid and default NAC will be used.*

5.2.2.7 Mode 6 - NVM Protection

Mode 6 is used to enable or disable the NVM Protection Mode by the given user-password. The header block for this working mode has the following structure:

The header block

00_H (Header Block)	**06_H** (Mode 6)	**Mode Data (5 bytes)**		**Checksum** (1 byte)
		User-password (1 byte)	**Not Used** (4 bytes)	

Mode Data Description

User-password: This Byte is given by user to enable or disable NVM protection mode.

Not used: The four Bytes are not used and will be ignored in mode 6.

In mode 6, the header block is the only transfer block to be sent by the host. If device is unprotected, the provided user-password will be set as NVM_PASSWORD and internally stored. No further commands will be accepted until a power up or hardware reset. Afterwards, protection mode will be enabled.

However, if the NVM is already protected, the microcontroller will deactivate the Protection and erase the NVM if the user-password Byte matches the stored NVM_PASSWORD Byte. If MSB of the NVM_PASSWORD is 0, only NVM Linearly mapped sectors are erased. If the Bit is 1, both NVM Linearly and Non-linearly mapped regions are erased. No further commands will be accepted until a power up or hardware reset. Afterwards, protection mode will be disabled.

In case NVM is protected and the given user-password does not match the stored NVM_PASSWORD, no actions will be triggered and a Protection Error (FD_H) will be returned instead of Acknowledge.

Note:

1. *Password value has to be different from 00_H and FF_H. If NVM_PASSWORD is set to either 00_H or FF_H on an unprotected device, the protection will not be set and a protection error (FD_H) will be returned.*
2. *When disabling NVM protection, together with NVM, the NAC and NAD values are erased too. As a result, after next reset, default NAD will be used and chip waits forever for the first Fast LIN BSL frame.*

Table 5-6 Erase NVM during unprotection

NVM_PASSWORD Bit 7	Description
0	Only linearly mapped NVM is erased.
1	Both linearly and non-linearly mapped NVM are erased.

5.2.2.8 Mode A - NVM Readout, Chip ID, Checksum

Mode A is used to get 4 Bytes Chip ID data, NVM or CS page read, NVM or CS page or NVM mass checksum check depending on the Option Byte value in the header block.

Different options are supported:

- Option 00_H: Get 4 Bytes Chip ID
- Option 10_H: NVM page checksum check
- Option 18_H: Mass NVM checksum check
- Option 50_H: Configuration sector page checksum check
- Option $C0_H$: NVM page read
- Option $F0_H$: Configuration sector page read

The header block for Get 4 Byte Chip ID (Option = 00_H)

00_H (Header Block)	**$0A_H$** (Mode A)	**Mode Data (5 bytes)**		**Checksum** (1 byte)
		Not Used (4 bytes)	**Option $=00_H$** (1 byte)	

Mode Data Description:

Not Used: These Bytes are not used and will be ignored for Option 00_H.

Option: Set to 00_H for Get 4 Byte Chip ID.

If this command is successfully received, microcontroller will return an Acknowledge followed by 4 data Bytes and a single byte checksum. The order of the 4 Bytes of data are SFR ID, CHIP_ID2, CHIP_ID1 and CHIP_ID0. Refer to **Chapter 6.2.1** for CHIP_ID definition.

Note: The checksum is calculated on the acknowledge and the 4 data bytes.

The header block for NVM page checksum check (Option = 10_H)

00_H (Header Block)	$0A_H$ (Mode A)	Data Area					Checksum (1 byte)
		StartAddr High (1 byte)	**StartAddr Low** (1 byte)	**Expected CHKSum High** (1 byte)	**Expected CHKSum Low** (1 byte)	**Option =10_H** (1 byte)	

Mode Data Description:

Start Addr High, Low: Address of the NVM page for checksum check. (Address should be page aligned).

Expected CHKSum High, Low: Expected checksum High/Low Byte.

Option: set to 10_H to enable NVM page checksum check.

Note: The start address provided with the header block has to be shifted by 7 bits to the left and then added to the NVM start address to build the actual address, i.e. it is calculated as follows in Mode A Option $C0_H$: Actual address = 11000000_H + (StartAddrHigh << 15) + (StartAddrLow << 7).

This option will trigger a checksum calculation (16 bits inverted XOR, refer to **Chapter 5.2.3**) over the whole page pointed by the address given in the header block and the result will then be compared with the expected checksum (provided as well by the user in the header frame). If the given address is a valid NVM address, the microcontroller will return an Acknowledge followed by four data Bytes and a single byte checksum. The Bytes are, in sequential order, pass/fail indication (00_H if the calculated and expected checksum match, 80_H if they differ), calculated checksum High Byte, calculated checksum Low Byte, and a final Byte equal to 00_H.

Note: The checksum is calculated on the acknowledge and the 4 data bytes.

The input address should always be page aligned. In case it is not aligned, the address will be internally changed to point to the beginning of the addressed page so that checksum is always evaluated on a complete page.

In case the provided address is not a valid NVM address, the microcontroller will return a Block Type Error (FF_H) instead of an Acknowledge (55_H) followed by no further Bytes.

Note: In case the address is pointing to an erased non linearly mapped page, the address is considered invalid and a Block Type Error (FF_H) is returned.

The header block for Mass checksum check (Option = 18_H)

00_H (Header Block)	$0A_H$ (Mode A)	Mode Data (5 bytes)					Checksum (1 byte)
		Not Used (1 byte)	**Not Used** (1 byte)	**Expected CHKSum High** (1 byte)	**Expected CHKSum Low** (1 byte)	**Option =18_H** (1 byte)	

Mode Data Description:

Not Used: These Bytes are not used and will be ignored for Option 18_H.

Expected CHKSum High, Low: Expected checksum High/Low Byte.

Option: set to 18_H to enable mass checksum check.

This option will trigger a checksum calculation (16 bits inverted XOR, refer to **Chapter 5.2.3**) over all the linearly mapped sectors not including the not linearly mapped sectors and CS pages. The result will then be compared with the expected checksum (provided by the user in the header frame). The microcontroller will return an Acknowledge followed by four data Bytes and a single byte checksum. The Bytes are, in sequential order, pass/fail indication (00_H if the calculated and expected checksum match, 80_H if they differ), calculated checksum High Byte, calculated checksum Low Byte, and a final Byte equal to 00_H.

Note: The checksum is calculated on the acknowledge and the 4 data bytes.

The header block for CS page checksum check (Option = 50_H)

00_H (Header Block)	$0A_H$ (Mode A)	Mode Data (5 bytes)					Checksum (1 byte)
		CS Page (1 byte)	**Not Used** (1 byte)	**Expected CHKSum High** (1 byte)	**Expected CHKSum Low** (1 byte)	**Option =50_H** (1 byte)	

Mode Data Description:

CS Page: Selection of the CS Page to be checked (refer to **Figure 6-2**).

Not Used: This Byte is not used and will be ignored for Option 50_H.

Expected CHKSum High, Low: Expected checksum High/Low Byte.

Option: set to 50_H to enable CS page checksum check.

This option will trigger a checksum calculation (16 bits inverted XOR, refer to **Chapter 5.2.3**) over the whole CS page pointed by the address given in the header block and the result will then be compared with the expected checksum (provided as well by the user in the header frame). CS page address has to be in accordance with the configuration sector address scheme described in the **Figure 6-2**. If the given address is valid, the microcontroller will return an Acknowledge followed by four data Bytes and a single byte checksum. The Bytes are, in sequential order, pass/fail indication (00_H if the calculated and expected checksum match, 80_H if they differ), calculated checksum High Byte, calculated checksum Low Byte, and a final Byte equal to 00_H.

In case the provided address is not valid, the microcontroller will return a Block Type Error (FF_H) instead of an Acknowledge (55_H) followed by no further Bytes.

Note: The checksum is calculated on the acknowledge and the 4 data bytes.

The header block for NVM page read (Option $C0_H$)

00_H (Header Block)	$0A_H$ (Mode A)	Mode Data (5 bytes)					Checksum (1 byte)
		StartAddr High (1 byte)	**StartAddr Low** (1 byte)	**Not Used** (1 byte)	**Not Used** (1 byte)	**Option =$C0_H$** (1 byte)	

Mode Data Description:

Start Addr High, Low: Address of the NVM page to be read (Address should be page aligned).

Not Used: These Bytes are not used and will be ignored for Option $C0_H$.

Option: set to $C0_H$ to enable NVM page read.

Note: The start address provided with the header block has to be shifted by 7 bits to the left and then added to the NVM start address to build the actual address, i.e. it is calculated as follows in Mode A Option $C0_H$: Actual address = 11000000_H + (StartAddrHigh << 15) + (StartAddrLow << 7).

This option will trigger a read of the addressed NVM page. Microcontroller will return an Acknowledge (55_H) followed by the 128 NVM page data Bytes (starting from the least significant Byte of the page).

The input address should always be aligned with a page. In case it is not aligned, the address will be internally changed to point to the beginning of the addressed page so that the page Bytes are always returned ordered from the least to the most significant Byte.

In case the provided address is not a valid NVM address, the microcontroller will return a Block Type Error (FF_H) instead of an Acknowledge (55_H) followed by no further Bytes.

To prevent user code to be read, this option is disabled if NVM is protected and only a Protection Error Byte (FD_H) will be returned.

Note: In case the address is pointing to an erased non linearly mapped page, the address is considered invalid and a Block Type Error (FF_H) is returned.

The header block for user configuration sector page read (Option = $F0_H$)

00_H (Header Block)	**$0A_H$** (Mode A)	**Mode Data (5 bytes)**					**Checksum** (1 byte)
		Not Used (1 byte)	**Not Used** (1 byte)	**Not Used** (1 byte)	**CS Page** (1 byte)	**Option =$F0_H$** (1 byte)	

Mode Data Description:

Not Used: These Bytes are not used and will be ignored for Option $F0_H$.

CS Page: Selection of the CS Page to be checked (refer to **Figure 6-2**).

Option: set to $F0_H$ to enable configuration sector page read.

This option will trigger a read of the addressed configuration sector page. Microcontroller will return an Acknowledge (55_H) followed by the 128 CS page data Bytes (starting from the least significant Byte of the page).

Configuration Sector page is selected by the CS Page Byte according to the scheme shown in **Figure 6-2**.

In case an invalid CS page is selected the microcontroller will return a Block Type Error (FF_H) instead of an Acknowledge (55_H) followed by no further Bytes.

To prevent user code to be read, this option is disabled if NVM is protected (NVM password installed) and only a Protection Error Byte (FD_H) will be returned.

All other values for option Byte

Block Type Error indication (FF_H) is sent back.

In mode A, the header block is the only transfer block to be sent by the host. The microcontroller will return an Acknowledge followed by data Bytes if the header block is received successfully. If an invalid option is received, the microcontroller will return a Block Type Error indication (FF_H) and no further Bytes.

5.2.3 16 bits inverted XOR checksum

This checksum structure is used in BSL Mode A options 10_H, 18_H, 50_H as a fast data integrity check. These modes will read the specified NVM range, calculate the checksum and compare it against the expected one provided as command parameter.

To calculate this checksum, all Half-Words (16 bits) of the selected NVM region are xored. The resulting value is then logically complemented (1´s complement).

The following figure shows the calculation algorithm.

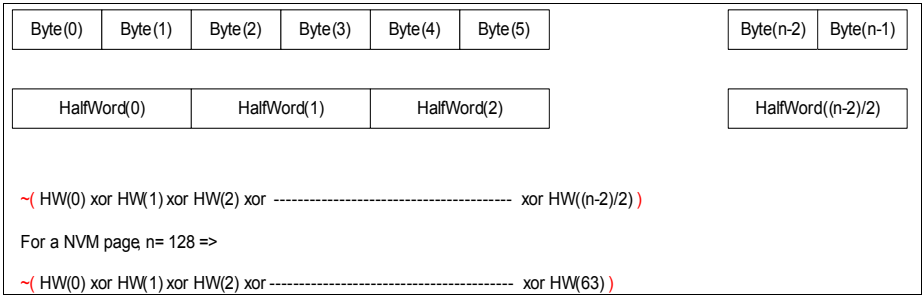

Figure 5-3 16 bits inverted XOR checksum calculation

5.3 WDT1 refreshing

After a reset the WDT1 is starting with a long open window. WDT1 keeps on running while waiting for first UART frame. In case during the UART BSL waiting time, defined by NAC, a UART communication is detected, WTD1 is disabled and its status frozen.

Subsequently, before exiting to RAM or NVM in UART BSL modes 1 and 3 the watchdog is re-enabled and starts from the previously frozen state. The WDT1 is then still in long open window and the remaining valid time is equal to long open window minus the time between reset release and first UART communication. User program needs to trigger the WDT1 refresh accordingly.

6 NVM

Non Volatile Memory (NVM) is the flash module of the TLE986xQX which partly supports EEPROM emulation.

6.1 NVM overview

The NVM is a single block of NVM memory of up to 128 kBytes separated into Code and Data space. The TLE986xQX device family provides products with different NVM sizes all sharing the same architecture and features. The following table shows the NVM address range.

Table 6-1 NVM address range

Address	Address Range
NSA to NEA	NVM memory

NSA and NEA values are shown in **Table 6-2**:

Table 6-2 NVM Size and Address Range

NVM Size (kB)	NVM Starting Address (NSA)	NVM Linear Size, NVM CFLASH Size (NLS)	NVM DFLASH Starting Address	NVM DFLASH Size	NVM DFLASH End Address, NVM FLASH End Address (NEA)
36	11000000_H	8000_H	11008000_H	1000_H	$11008FFF_H$
64	11000000_H	$F000_H$	$1100F000_H$	1000_H	$1100FFFF_H$
128	11000000_H	$1F000_H$	$1101F000_H$	1000_H	$1101FFFF_H$

Note: An erased page is ECC-Clean and will not generate an ECC error.

Note: Reading an erased page in the Code space will return FF_H and will not trigger any error on the AHB Lite bus (HRESP[1] = 00_B).

Note: Reading an erased page in the Data space will return 00_H and will trigger an error on the AHB Lite bus (HRESP[1] = 01_B). This will also create an NVM Map Error NMI, if enabled in NMICON, in addition to the hard fault. As a consequence, an erased page in the Data space has to be written before it can be read without triggering an error.

1) refer to Cortex M3 Integration and Implementation Manual revision r2p1.

6.1.1 NVM organisation

The NVM has 2 types of memory configuration, Code and Data. It is organised in sectors. Each NVM Sector is a block of 4 kBytes organised into blocks of 128 Bytes called Page. The page is the minimum data granularity for NVM (code and data) write and erase so, with this NVM structure, any NVM update, even when targeting only one byte, actually involves 128 bytes. **Table 6-3** shows the sector address organisation of 128 kBytes NVM. Sector organization for other NVM sizes can be simply derived per extension of the reported scheme. **Table 6-4** shows the page address organisation of NVM Sector 1 and it can be used as a reference for page organization of any NVM Sector.

Table 6-3 NVM memory sector organisation

Address	NVM Sector Number
11000000H to 11000FFFH	1
11001000H to 11001FFFH	2
11002000H to 11002FFFH	3
11003000H to 11003FFFH	4
11004000H to 11004FFFH	5
11005000H to 11005FFFH	6
11006000H to 11006FFFH	7
11007000H to 11007FFFH	8
11008000H to 11008FFFH	9
11009000H to 11009FFFH	10
1100A000H to 1100AFFFH	11
1100B000H to 1100BFFFH	12
1100C000H to 1100CFFFH	13

Table 6-3 NVM memory sector organisation (cont'd)

Address	NVM Sector Number
1100D000H to 1100DFFFH	14
1100E000H to 1100EFFFH	15
1100F000H to 1100FFFFH	16
11010000H to 11010FFFH	17
11011000H to 11011FFFH	18
11012000H to 11012FFFH	19
11013000H to 11013FFFH	20
11004000H to 11004FFFH	21
11015000H to 11015FFFH	22
11016000H to 11016FFFH	23
11017000H to 11017FFFH	24
11018000H to 11018FFFH	25
11019000H to 11019FFFH	26
1101A000H to 1101AFFFH	27
1101B000H to 1101BFFFH	28
1101C000H to 1101CFFFH	29
1101D000H to 1101DFFFH	30

Table 6-3 NVM memory sector organisation (cont'd)

Address	NVM Sector Number
1101E000H to 1101EFFFH	31
1101F000H to 1101FFFFH	32

Table 6-4 NVM memory sector 1 page organisation

Address	Page Number of NVM Sector
11000000H to 1100007FH	0
11000080H to 110000FFH	1
11000100H to 1100017FH	2
11000180H to 110001FFH	3
11000200H to 1100027FH	4
11000280H to 110002FFH	5
11000300H to 1100037FH	6
11000380H to 110003FFH	7
11000400H to 1100047FH	8
11000480H to 110004FFH	9
11000500H to 1100057FH	10
11000580H to 110005FFH	11
11000600H to 1100067FH	12

Table 6-4 NVM memory sector 1 page organisation (cont'd)

Address	Page Number of NVM Sector
11000680H to 110006FFH	13
11000700H to 1100077FH	14
11000780H to 110007FFH	15
11000800H to 1100087FH	16
11000880H to 110008FFH	17
11000900H to 1100097FH	18
11000980H to 110009FFH	19
11000A00H to 11000A7FH	20
11000A80H to 11000AFFH	21
11000B00H to 11000B7FH	22
11000B80H to 11000BFFH	23
11000C00H to 11000C7FH	24
11000C80H to 11000CFFH	25
11000D00H to 11000D7FH	26
11000D80H to 11000DFFH	27
11000E00H to 11000E7FH	28
11000E80H to 11000EFFH	29

Table 6-4 NVM memory sector 1 page organisation (cont'd)

Address	Page Number of NVM Sector
11000F00H to 11000F7FH	30
11000F80H to 11000FFFH	31

6.2 NVM configuration sectors organisation

The configuration sector contains important user data needed for proper system initialization.

6.2.1 Chip ID definition

The specific characteristics of the different variants of the product family are captured in the definition of the CHIP_ID Bytes.

The Chip_ID bytes can be read via BSL mode A. When triggered, this mode replies providing the 3 CHIP_ID Bytes plus the content of the Identification Register (ID).

Please refer to the following tables for CHIP_ID details. This is a variant specific identification number. The unique device specific identification number is described in **Table 6-11**.

Table 6-5 Chip ID Byte 0

Res	MAX_FREQ	OP_AMP	Phases	DMA	PKG Type

Table 6-6 Chip ID Byte 0 Bits Description

Field	Bits	Description
PKG_Type	[1:0]	Package Type 00 VQFN-48 01 Reserved 10 Reserved 11 Reserved
DMA	2	DMA 0 with DMA 1 without DMA
Phases	3	Bridge driver number of phases 0 2 phases 1 3 phases

Table 6-6 Chip ID Byte 0 Bits Description

Field	Bits	Description
OP_AMP	4	Op Amp 0 with Op Amp 1 without Op Amp
Max Freq	[6:5]	Maximum Frequency 00 reserved 01 20 MHz 10 24MHz 11 40 MHz
Res	7	Reserved

Table 6-7 Chip ID Byte 1

NVM_SIZE	EEPROM_SIZE

Table 6-8 Chip ID Byte 1 Bits Description

Field	Bits	Description
EEPROM_SIZE	[3:0]	EEPROM (Non-linearly Mapped NVM) Size 0000 0 Kbyte 0001 4 Kbyte 0010 8 Kbyte 0011 12 Kbyte 0100 16 Kbyte 0101 20 Kbyte 0110 24 Kbyte 0111 28 Kbyte 1000 32 Kbyte 1001 36 kByte 1010 40 Kbyte 1011 44 Kbyte 1100 48 Kbyte 1101 52 Kbyte 1110 56 Kbyte 1111 60 Kbyte
NVM_SIZE	[7:4]	Linearly Mapped NVM Size 0000 24 Kbyte 0001 28 Kbyte 0010 32 Kbyte 0011 36 Kbyte 0100 52 Kbyte 0101 56 Kbyte 0110 60 Kbyte 0111 64 Kbyte 1000 84 Kbyte 1001 88 kByte 1010 92 Kbyte 1011 96 Kbyte 1100 116 Kbyte 1101 120 Kbyte 1110 124 Kbyte 1111 128 Kbyte

Table 6-9 Chip ID Byte 2

Res	RAM_ID	VARIANT_ID

Table 6-10 Chip ID Byte 2 Bits Description

Field	Bits	Description
VARIANT_ID	[3:0]	Variant ID
RAM_ID	[5:4]	RAM ID 00 3kB 01 4kB 10 6kB 11 3kB
Res	[7:6]	Reserved

6.2.2 100 Time Programmable data

User has eight 100 time programmable pages. The first one is used to store user configuration parameters for measurement interface and sense amplifier as well as ADC1 calibration parameters. These parameters are usually determined in the user application and might require several iterations before the best fit is found.

The values of the first page, from offset 10_H to 63_H, are automatically copied into the dedicated SFR registers after every power on reset, brown out reset or wake-up reset from sleep mode thus replacing the registers default reset values. The user can check them by reading the dedicated SFRs or by reading directly the content of the page.

The first 4 Bytes of the first 100TP page are used to store a device ID that can be read by the user. The content of these 4 bytes are preloaded prior to shipment and cannot be modified by the user. In case the user tries to write these values via the 100TP page writing features offered in BSL or via NVM user routine, an error is reported and the original content of the bytes is preserved. The Customer_ID definition is described in **Figure 6-1**.

The data stored in this first 100 time programmable page can be found in **Table 6-11**.

To read data stored in the 100TP pages, refer to **Section 6.3.10**.

To perform the programming of these pages, the user is required to preload the contents to be programmed into the RAM as listed in **Table 6-12**. The offset entered for the programming does not need to be in sequential order. Once a page has been programmed 100 times, no further programming on that page is allowed. In the last Byte of each 100TP page a program counter is stored (not changeable by user).

For further information regarding 100TP page program, refer to **Section 6.3.11**.

Table 6-11 100-Time Programmable Page 1

Data Offset	SFR / Variable Name	Description	Default Value
00_H to 03_H	CUSTOMER_ID	Device ID for user	Device ID dependent
04_H	GAIN_VS_10B	Calibration gain for supply voltage measurement	Chip Individual
05_H	OFFSET_VS_10B	Calibration offset for supply voltage measurement	Chip Individual
06_H	GAIN_VBAT_SENSE_10B	Calibration gain for battery voltage measurement	Chip Individual
07_H	OFFSET_VBAT_SENSE_10B	Calibration offset for battery voltage measurement	Chip Individual
08_H	GAIN_VMON_ATT_1_5	Calibration gain for high voltage monitoring input voltage measurement	Chip Individual
09_H	OFFSET_VMON_ATT_1_5	Calibration offset for high voltage monitoring input voltage measurement	Chip Individual
$0A_H$	CONFIG_VERS	Configuration Sector version	02_H
$0B_H$	Reserved	Reserved	00_H
$0C_H$ to $0D_H$	CFLASH_PW	Linearly mapped region protection removal password	0000_H
$0E_H$ to $0F_H$	DFLASH_PW	Non-Linearly mapped region protection removal password	0000_H
10_H to 13_H	MEAS_ADC2_CTRL1	Measurement unit: Control register 1	00000000_H
14_H to 17_H	MEAS_ADC2_CTRL2	Measurement unit: Control register 2	00000703_H
18_H to $1B_H$	MEAS_ADC2_SQ1_4	Channel controller: Measurement channel enable Bits of cycle 1 to 4	29362837_H
$1C_H$ to $1F_H$	MEAS_ADC2_SQ5_8	Channel controller: Measurement channel enable Bits of cycle 5 to 8	28372836_H

Table 6-11 100-Time Programmable Page 1 (cont'd)

Data Offset	SFR / Variable Name	Description	Default Value
20_H to 23_H	MEAS_ADC2_SQ9_10	Channel controller: Measurement channel enable Bits of cycle 9 to 10	00002936_H
24_H to 27_H	ADC2_CAL_CH0_1	Calibration unit: Calibration of channel 0 and 1	Chip Individual
28_H to $2B_H$	ADC2_CAL_CH2_3	Calibration unit: Calibration of channel 2 and 3	Chip Individual
$2C_H$ to $2F_H$	ADC2_CAL_CH4_5	Calibration unit: Calibration of channel 4 and 5	Chip Individual
30_H to 33_H	ADC2_FILTCOEFF0_5	IIR filter: Filter coefficients of ADC channels 0 to 5	$00000AAA_H$
34_H to 37_H	ADC2_FILT_UP_CTRL	Postprocessing: Upper threshold filter enable	$00000F3F_H$
38_H to $3B_H$	ADC2_FILT_LOW_CTRL	Postprocessing: Lower threshold filter enable	$00000F3F_H$
$3C_H$ to $3F_H$	ADC2_TH0_3_LOWER	Postprocessing: Lower comparator trigger level of channels 0 to 3	$182F423A_H$
40_H to 43_H	ADC2_TH4_5_LOWER	Postprocessing: Lower comparator trigger level of channels 4 to 5	$00009A00_H$
44_H to 47_H	ADC2_TH6_9_LOWER	Postprocessing: Lower comparator trigger level of channels 6 to 9	$C6D339CD_H$
48_H to $4B_H$	ADC2_TH0_3_UPPER	Postprocessing: Upper comparator trigger level of channels 0 to 3	$ABBDC5C0_H$
$4C_H$ to $4F_H$	ADC2_TH4_5_UPPER	Postprocessing: Upper comparator trigger level of channels 4 to 5	$0000BC00_H$
50_H to 53_H	ADC2_CNT0_3_LOWER	Postprocessing: Lower counter trigger level of channels 0 to 3	12131312_H

Table 6-11 100-Time Programmable Page 1 (cont'd)

Data Offset	SFR / Variable Name	Description	Default Value
54_H to 57_H	ADC2_CNT4_5_LOWER	Postprocessing: Lower counter trigger level of channels 4 to 5	$00000A0A_H$
58_H to $5B_H$	ADC2_CNT0_3_UPPER	Postprocessing: Upper counter trigger level of channels 0 to 3	$12131B1A_H$
$5C_H$ to $5F_H$	ADC2_CNT4_5_UPPER	Postprocessing: Upper counter trigger level of channels 4 to 5	00001212_H
60_H to 63_H	ADC2_MMODE0_5	Postprocessing: Overvoltage measurement mode of channels 0 to 5	00000000_H
64_H to $6B_H$	Reserved	Reserved	00_H
$6C_H$	CHIP_ID_BYTE_00	Chip Id Byte 00[1)]	Chip Individual
$6D_H$	CHIP_ID_BYTE_01	Chip Id Byte 01[1)]	Chip Individual
$6E_H$	CHIP_ID_BYTE_02	Chip Id Byte 02[1)]	Chip Individual
$6F_H$	CHIP_ID_BYTE_03	Chip Id Byte 03[1)]	Chip Individual
70_H	CHIP_ID_BYTE_04	Chip Id Byte 04[1)]	Chip Individual
71_H	CHIP_ID_BYTE_05	Chip Id Byte 05[1)]	Chip Individual
72_H	CHIP_ID_BYTE_06	Chip Id Byte 06[1)]	Chip Individual
73_H	CHIP_ID_BYTE_07	Chip Id Byte 07[1)]	Chip Individual
74_H	CHIP_ID_BYTE_08	Chip Id Byte 08[1)]	Chip Individual
75_H	CHIP_ID_BYTE_09	Chip Id Byte 09[1)]	Chip Individual

Table 6-11 100-Time Programmable Page 1 (cont'd)

Data Offset	SFR / Variable Name	Description	Default Value
76_H	CHIP_ID_BYTE_10	Chip Id Byte 10[1)]	Chip Individual
77_H	CHIP_ID_BYTE_11	Chip Id Byte 11[1)]	Chip Individual
78_H	CS_SA_WITH_PROT_EN	When set to $A5_H$, enables Service Algorithm even on protected NVM Data Sector.	00_H
79_H	CS_USER_CAL_STARTUP_EN	Enable Byte for user calibration data download during startup. If value=0xC3 then the download is enabled	00_H
$7A_H$	CS_USER_CAL_XADDH	High Byte of the RAM starting address where downloaded data has to be stored(0xF0 for RAM initial address)	00_H
$7B_H$	CS_USER_CAL_XADDL	LOW Byte of the RAM starting address where downloaded data has to be stored(0x00 for RAM initial address)	00_H
$7C_H$	CS_USER_CAL_CS_PAGE	CS page where calibration data has to be downloaded from. By default 100TP page1 should be used (Value=0x11)	00_H
$7D_H$	CS_USER_CAL_NUM	Number of Bytes to be downloaded starting from the first Byte of the selected CS page.	00_H
$7E_H$	CHECKSUM_S0_P29	Checksum_S0_P29, XOR first 126 Bytes of page 29	Chip Individual
$7F_H$	PROG_TIMES_100TP_P1	This reflects the number of times that this page has been programmed. (Up to a maximum of 100 times.)	00_H

1) This is a unique device specific identification number. The variant specific identification number is described in **Chapter 6.2.1**.

Table 6-12 RAM preloading for 100 Time Programmable page programming

RAM Address	Function
18000400_H	Number of Bytes to be programmed (i.e. **N**, up to a maximum of 127[1)] Bytes)
18000401_H	100TP offset 1
18000402_H	100TP data 1 to be programmed
18000403_H	100TP offset 2
18000404_H	100TP data 2 to be programmed
.....	....
18000401_H + ((N-1) x 2)	100TP offset N
18000402_H + ((N-1) x 2)	100TP data N to be programmed

1) The maximum number of bytes that the user can load into the 100TP pages is limited to 127 since last byte is used as a program operation counter. To ensure that the page are not programmed more than 100 times, even not by accident, the counter byte (last byte in the page) can be read but not overwritten by the user.

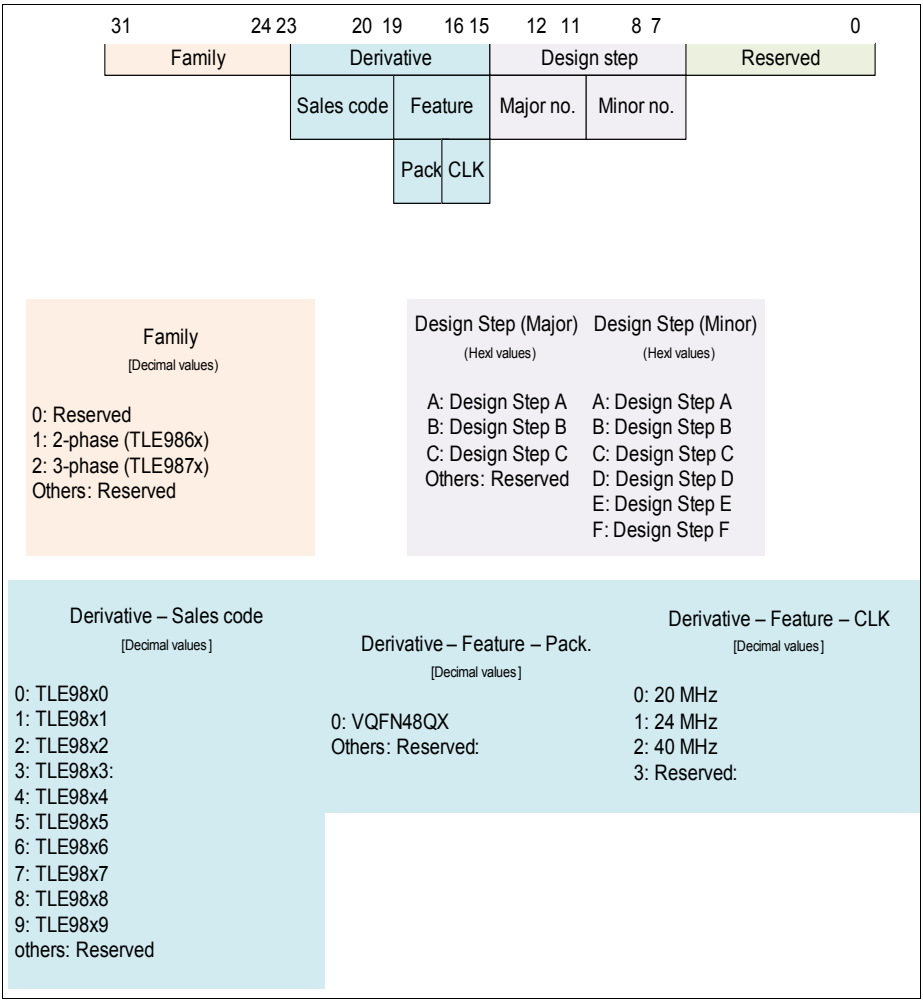

Figure 6-1 Customer_ID definition

6.3 NVM user routines organisation

The NVM user routines are BootROM routines called by user and placed from the address $0000383D_H$ to 00003925_H. The complete list of NVM user routines can be found in **Table 6-13**.

Table 6-13 NVM user routines list

Address	Routine	Description
00003925_H	USER_CFLASH_WR_PROT_EN	To enable write protection on the linearly mapped NVM sectors.
$0000391D_H$	USER_CFLASH_WR_PROT_DIS	To disable write protection on the linearly mapped NVM sectors.
00003915_H	USER_CFLASH_RD_PROT_EN	To enable read protection on the linearly mapped NVM sectors.
$0000390D_H$	USER_CFLASH_RD_PROT_DIS	To disable read protection on the linearly mapped NVM sectors.
00003905_H	USER_DFLASH_WR_PROT_EN	To enable write protection on the non linearly mapped NVM sectors.
$000038FD_H$	USER_DFLASH_WR_PROT_DIS	To disable write protection on the non linearly mapped NVM sectors.
$000038F5_H$	USER_DFLASH_RD_PROT_EN	To enable read protection on the non linearly mapped NVM sectors.
$000038ED_H$	USER_DFLASH_RD_PROT_DIS	To disable read protection on the non linearly mapped NVM sectors.
$000038E5_H$	USER_OPENAB	To open the assembly buffer for writing
$000038DD_H$	USER_PROG	To program the NVM
$000038D5_H$	USER_ERASEPG	To erase an NVM page
$000038CD_H$	USER_ABORTPROG	To abort the NVM programming by closing the assembly buffer
$000038C5_H$	USER_NVMRDY	To access if the NVM is in ready to read status
$000038BD_H$	USER_READ_CAL	To read the NVM calibration data.
$000038B5_H$	USER_NVM_CONFIG	To read the NVM configuration status

Table 6-13 NVM user routines list (cont'd)

Address	Routine	Description
$000038AD_H$	USER_NVM_ECC2ADDR	To read the NVM ECC2 address
$0000389D_H$	USER_MAPRAM_INIT	To initialize MapRAM
00003875_H	USER_READ_100TP	To read the NVM 100TP parameter data
$0000386D_H$	USER_100TP_PROG	To perform the 100TP program. (This can be used 100 times per 100TP page)
00003865_H	USER_ERASE_SECTOR	To erase an NVM Sector
00003855H	USER_NVMCLKFAC_SET	To set NVMCLKFAC Bit in SYSCON0
$0000384D_H$	USER_RAM_MBIST_START	To perform a sequential checkerboard and inverted checkerboard test on the RAM.
00003845_H	USER_NVM_ECC_CHECK	To trigger a complete NVM read and provide cumulated ECC single bit error indication.
$0000383D_H$	USER_ECC_CHECK	To provide cumulated ECC single bit error indication since last call of the function.

Table 6-14 NVM User Routines Maximum Stack Usage

Routine	Maximum Stack Usage
USER_CFLASH_WR_PROT_EN	0000_H
USER_CFLASH_WR_PROT_DIS	0000_H
USER_CFLASH_RD_PROT_EN	0000_H
USER_CFLASH_RD_PROT_DIS	0000_H
USER_DFLASH_WR_PROT_EN	0000_H
USER_DFLASH_WR_PROT_DIS	0000_H
USER_DFLASH_RD_PROT_EN	0000_H
USER_DFLASH_RD_PROT_DIS	0000_H
USER_OPENAB	0038_H
USER_PROG	$00B0_H$
USER_ERASEPG	0040_H

Table 6-14 NVM User Routines Maximum Stack Usage (cont'd)

Routine	Maximum Stack Usage
USER_ABORTPROG	0010_H
USER_NVMRDY	0000_H
USER_READ_CAL	0030_H
USER_NVM_CONFIG	$000C_H$
USER_NVM_ECC2ADDR	$000C_H$
USER_MAPRAM_INIT	0010_H
USER_READ_100TP	0030_H
USER_100TP_PROG	0084_H
USER_ERASE_SECTOR	0030_H
USER_SET_USER_CLK	0030_H
USER_NVMCLKFAC_SET	0008_H
USER_RAM_MBIST_START	$01D0_H$
USER_NVM_ECC_CHECK	0020_H
USER_ECC_CHECK	0020_H

6.3.1 Opening assembly buffer routine

The NVM programming routine consists of two parts: The assembly buffer opening routine, and the programming and verification routine.

The Open Assembly buffer routine reads the content of the physical page into a NVM internal RAM memory block (Assembly Buffer). The address of the page to be read is provided with the OpenAB function call. Once the OpenAB call has been executed successfully the user can update the content of the Assembly Buffer (128 bytes) by (over)writing the data starting from the address handed over to the OpenAB function.

In case the provided address targets the NVM data region, before copying the data, the OpenAB routine will check to which physical page the provided address is linked to and make the data of this physical page available into the Assembly Buffer.

Note: The assembly buffer opening routine needs to be executed successfully before the NVM programming routine can be called.

Table 6-15 Opening assembly buffer subroutine

Subroutine	**000038E5$_H$: USER_OPENAB** Prototype: char **USER_OPENAB**(unsigned int *address)
Input	***Address(integer pointer)**: pointer to the NVM address to be programmed
Output	**Return value (char):** Bit 0: Pass or fail 0 = Assembly Buffer is successfully opened 1 = Assembly Buffer cannot be opened. Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reasons of failure: - Corrupted NVM data sector. - The range of the address is protected. - The range of the address is incorrect. Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching) - Assembly Buffer is already opened.

Once assembly buffer is opened, user must either proceed with the standard program flow (refer to **Figure 6-9**) or close the assembly buffer using the dedicated abort programming user routine (refer to **Chapter 6.3.4**). All other sequences are not allowed and might lead to loss of data.

6.3.2 NVM programming routine

There are 2 types of programming available, Type 1 or Type 2 (Type 1 without or Type 2 with RAM background activity during NVM operation).

For Type 1 programming, the flow control is always kept by the BootROM NVM programming routine. Consequently, no other operations can be run in parallel thus avoiding making use of the NVM operation waiting time. In Type 2 programming, the BootROM routine starts the write operation and then gives back control to the user software by branching to the RAM address 18000400$_H$. In this scenario, the user software needs to reside in RAM because no access to the NVM is possible while

internal program sequence is on-going. The user software needs to hand back the control to the NVM programming routine, which continues with polling the busy Bit.

A description of the BootROM programming routine is provided in the following **Table 6-16**. More information on the support for background activity during NVM operation can be found in **Section 6.4.2**.

The program operation is executed on the page selected by the previously called USER_OPENAB. In case the target page belongs to the NVM Data region, at the end of a successful program operation, the USER_PROG routine properly updates the MapRAM information mapping the page just written and randomly selects a proper spare page between the available (not written and not faulty) pages. In case, for any reason, a valid spare page cannot be found, the routine returns a proper error indication. In such case all data previously written, including the page just written is still accessible (no data loss).

Table 6-16 Programming subroutine

Subroutine	**$000038DD_H$: USER_PROG** Prototype: char **USER_PROG**(char PROG_FLAG)

Table 6-16 Programming subroutine (cont'd)

Input	**PROG_FLAG (char)**: Byte for controlling the programing routine. Bit 0: RAM branching control bit 0 = RAM branching disabled 1 = RAM branching enabled Bit 1: Corrective action (retry and disturb handling) control bit 0 = Corrective actions disabled 1 = Corrective actions enabled Bit 2: Failing page erase control bit when addressing non linearly mapped sector (refer to **Chapter 6.4.4.2** for more details) 0 = Failing page erase enabled. The programmed data are erased in case of fail. If the page was already used, old data are kept. 1 = Failing page erase disabled. Programmed data are not erased in case of fail. If page was already used, old data are not kept and the new failing data are accessible by reading the target page.

Table 6-16 Programming subroutine (cont'd)

Output	**Return value (char):** Bit 0 Pass or Fail.This bit is the OR of the bits 4, 5, 6 and 7 0 = Programming completed successfully. No errors occurred 1 = Programming failed. At least one error occurred Bit 1-3: Reserved Bit 4: Verify Pass/Fail 0 = Pass: The verification of the programmed data passed 1 = Fail: The verification of the programmed data failed Bit 5: Emergency Operation Pass/Fail 0 = Pass: The normal flow of the program operation has not been interrupted by an emergency operation request. 1 = Fail: The normal flow of the program operation has not been completed due to a request of an emergency operation Bit 6: Spare page selection Pass/Fail (Valid only for operation run on NVM Data pages) 0 = Pass: A new random spare page has been properly selected 1 = Fail: The random spare page selection failed. No random spare page selected Bit 7: Execution Pass/Fail status 0 = Pass: Routine execution could be properly started 1 = Fail: Routine execution could not be properly started due to missing required setting (Assembly Buffer not opened, target region write protected, nested call execution) Note: No NVM prog or erase routine can be called until this NVM operation is completed.

6.3.3 NVM page erasing routine

Similarly, there are 2 types of erasing available, Type 1 or Type 2 (Type 1 without or Type 2 with RAM background activity during NVM operation). Details in the following table.

Table 6-17 Page erasing subroutine

Subroutine	**000038D5$_H$: USER_ERASEPG** Prototype: char **USER_ERASEPG**(unsigned int *NVMPageAddr, char RAM_RTNE_BRNCHNG)
Input	***NVMPageAddr (integer pointer)**: pointer to the NVM address to be erased RAM_RTNE_BRNCHNG **(char)**: To enable or disable background execution from RAM. Bit 0: RAM branching control bit 0 = RAM branching disabled 1 = RAM branching enabled
Output	**Return value (char):** Bit 0: Pass or Fail 0 = Erasing completed successfully. 1 = Erasing failed. Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reasons of failure: - The range of the address is incorrect. - This is a protected range. Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching) Note: No NVM prog or erase routine can be called until this NVM operation is completed.

6.3.4 Abort NVM programming routine

This user routine aborts the NVM programming by closing an opened assembly buffer.

Table 6-18 Abort NVM programming subroutine

Subroutine	**000038CD$_H$: USER_ABORTPROG** Prototype: bool **USER_ABORTPROG**(void)
Input	--
Output	**Return value (bool): Pass or Fail** 0 = Abort successfully, assembly buffer closed. 1 = Abort failed as programming already started. Possible reason of failure: - Programming already started. - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching)

6.3.5 Read NVM status routine

This user routine checks for the NVM status.

Table 6-19 Read NVM status subroutine

Subroutine	**000038C5$_H$: USER_NVMRDY** Prototype: bool **USER_NVMRDY**(void)
Input	--
Output	**Return value (bool): Pass or Fail** 0 = NVM is not busy. 1 = NVM is busy now.

6.3.6 Read user calibration data

All data stored in user accessible config sector pages (100TP) can be downloaded into the RAM using this routine. In particular, this routine has been developed to help user in downloading the ADC1 calibration parameters stored at the beginning of 100TP page 1 (See **Table 6-11**) to an easily accessible data space (RAM). To download the data, the user needs to provide the config sector page where data has to be read from, number of Bytes to be copied, and the RAM address where data has to be copied to. The routine will copy the specified number of Bytes from the selected page (starting always from first Byte in the page) into the RAM (starting at the given address).

Note: The provided RAM address where data have to be copied is just an offset to the device RAM start address (18000000$_H$).

Table 6-20 Read user calibration data subroutine

Subroutine	**000038BD$_H$: USER_READ_CAL** Prototype: char **USER_READ_CAL**(char NumOfBytes, char CSAddr, short RAMAddr)
Input	**NumOfBytes (char)**: Number of Bytes to be copied from config sector into the RAM (allowed values are form 01$_H$ to 80$_H$). **CSAddr (char)**: user CS page to take data from (refer to **Figure 6-2**). **RAMAddr (short)**: RAM address offset to copy data to (03FF$_H$ < RAMAddr < RAMAddr + NumOfBytes < RAM size). RAM size: 3 kB RAM: 0BFF$_H$ 6 kB RAM: 17FF$_H$
Output	**Return value (char):** Bit 0: Pass or Fail 0 = Read is successful. 1 = Read is not successful due to invalid input values. Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reasons of failure: - The input parameters are incorrect. Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching)

6.3.7 Read NVM config status routine

This routine reads the NVM Configuration Status. Details in the following table.

Table 6-21 Read NVM config status subroutine

Subroutine	**000038B5$_H$: USER_NVM_CONFIG** Prototype: bool **USER_NVM_CONFIG**(char *NVMSize, char *MapRAMSize)
Input	--
Output	**Return value (bool): Pass or fail** 0 = Configuration read successfully. 1 = Configuration read failed. **NVMSize (char pointer):** pointer to the RAM location where the number of available sectors of the code area (4 kBytes each) has to be saved **MapRAMSize (char pointer)**: pointer to the RAM location where to store the number of available sectors of the data area (4 kBytes each) Possible reason of failure: - NVM Linear sector is set as 00$_H$.

6.3.8 Read NVM ECC2 address routine

This routine returns the result of the last NVM address accessed resulting in a double ECC error. Details in the following table.

Table 6-22 Read NVM ECC2 address subroutine

Subroutine	**000038AD$_H$: USER_NVM_ECC2ADDR** Prototype: char **USER_NVM_ECC2ADDR**(unsigned int *ECC2Addr)

Table 6-22 Read NVM ECC2 address subroutine (cont'd)

Input	**ECC2Addr (unsigned short pointer):** Pointer to the RAM location where the last NVM address with ECC2 error shall be stored
Output	**Returned Value (char):** Bit 0: ECC2 error detection 0 = No NVM ECC2 detected 1 = NVM ECC2 address detected Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reason for execution fail: - Null pointer passed to the routine - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching)

The address reported as an output in the RAM location is passed as a pointer. The returned value always provides the starting address of the 8 Byte section where the ECC error happened.

6.3.9 MapRAM initialization

This routine is meant to be used to re-initialize the MapRAM. The routine performs a complete MapRAM initialization by triggering a dedicated function of the NVM internal Finite State Machine. When triggered, the state machine resets the whole MapRAM and rebuilds information by reading the current logical to physical address information stored directly into the NVM data sector. In case of mapping errors (double or multiple mapping or faulty pages) the initialization of the MapRAM is stopped on the first error found and the routine is exited reporting a proper error indication. In case of fail, the content of the MapRAM might be only partial and the mapping information might be corrupted.

The routine can be used to try to restore a clean MapRAM status in case a MapRAM error has been reported by the startup or by the program routine or in case some data sector pages have been lost. In addition, this routine can be used to check whether the mapped sector has a consistent status.

Note: In case an NVM operation on the Data region is interrupted (e.g. due to reset events), the mapped sector might have an inconsistent status depending on the moment in which the interruption occurred. In case of power-on reset, brown-out reset, pin reset or wake-up reset the system performs the MapRAM initialisation during the following startup and triggers the Service Algorithm to try to repair mapping inconsistency, if required. The user shall then check the status of the mapped region evaluating the information

reported on the MEMSTAT and SYS_STRTUP_STS registers. In case of software reset (e.g. issued during a RAM branching) or internal watchdog reset, the following startup sequence does not perform any check of the mapped sector. In this case the user shall trigger the USER_MAPRAM_INIT function in the application code before performing any other NVM operation to check the presence of inconsistent mapping in the NVM Data region.

Table 6-23 MapRAM initialization subroutine

Subroutine	**0000389D$_H$: USER_MAPRAM_INIT** Prototype: char **USER_MAPRAM_INIT**(void)
Input	--
Output	**Return value (char):** Bit 0: Pass or Fail. It is the OR of the bits 5, 6 and 7 0 = MapRAM initialization pass 1 = MapRAM initialization fail Bit 1 to 4: Reserved Bit 5: Double mapping 0 = Pass: No double mapping found 1 = Fail: The initialization failed due to double mapping Bit 6: Faulty page 0 = Pass: No faulty pages found 1 = Fail: The initialization failed due to faulty page Bit 7: Execution Pass/Fail status 0 = Pass: Routine execution could be properly started 1 = Fail: Routine execution could not be properly started due to missing required setting (e.g.: Opened Assembly Buffer, nested call execution) Note: No NVM prog or erase routine can be called until this NVM operation is completed.

6.3.10 Read 100 Time Programmable parameter data routine

This routine reads the 100TP page content. For the 100TP page 1, the data offset range is listed in **Table 6-11**. Details in the following table.

Table 6-24 Read 100 Time Programmable subroutine

Subroutine	**00003875_H: USER_READ_100TP** Prototype: bool **USER_READ_100TP**(char 100TP_Page_Sel, unsigned char DataOffset, int *HundredTPData)
Input	**100TP_Page_Sel (char)**: 100TP page selection Byte (CS_Byte, refer to **Figure 6-2**) **DataOffset (unsigned char)**: Data Offset in page (00_H to $7F_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Read is successful. 1 = Read is not successful due to invalid range selected. **HundredTPData (integer pointer)** = Pointer to the RAM location where 100TP Data is saved

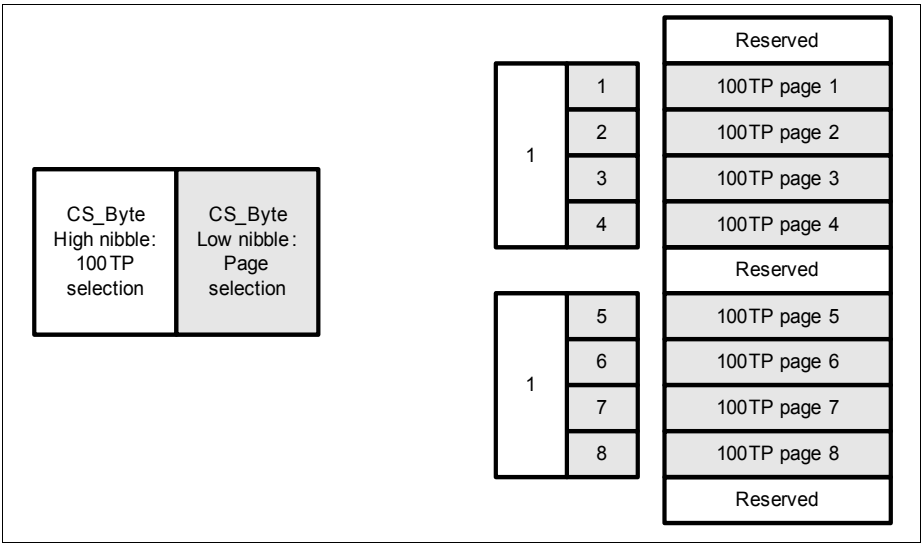

Figure 6-2 User configuration sector pages address Byte description

6.3.11 Program 100 Time Programmable routine

This routine programs data into the 100TP pages. The 100TP content to be programmed has to be preloaded into the RAM. The details can be found in **Section 6.2.2**.

Table 6-25 Program 100 Time Programmable subroutine

Subroutine	**0000386D$_H$: USER_100TP_PROG** Prototype: char **USER_100TP_PROG**(char 100TP_Page_Sel)
Input	**100TP_Page_Sel (char):** 100TP page selection Byte (CS_Byte, refer to **Figure 6-2**) RAM preloaded with the 100TP data to be programmed.
Output	**Returned value (char):** Bit 0: Program operation pass or fail flag 0 = Program completed successfully 1 = Program failed. Bit 1: In page offset error flag 0 = All bytes have in page offset 1 = At least one byte has a not in page offset. Note: not in page bytes are not programmed and do not result in a program error on bit 0. Note: Counter position is already considered out of range Bit 2: ID protected region fail flag 0 = All bytes do not target the reserved Customer_ID region 1 = At least 1 Byte targets the reserved Customer_ID region Note: Bytes targeting the Customer_ID region are not programmed and do not result in a program fail error on bit 0 Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reasons of failure: - The NVM code area is protected against programming. - The 100TP page is already programmed to a maximum of 100 times. Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching) Note: No NVM prog or erase routine can be called until this NVM operation is completed.

6.3.12 Sector Erasing Routine

This routine is used to perform an erase of a NVM data sector.

Table 6-26 Sector Erasing Subroutine

Subroutine	**00003865_H: USER_ERASE_SECTOR** Prototype: char **USER_ERASE_SECTOR**(unsigned int sectorAddress)
Input	**SectorAddress (unsigned int)**: NVM Sector address
Output	**Returned value (char):** Bit 0: Pass or Fail 0 = Erasing completed successfully. 1 = Erasing failed. Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via RAM branching) Note: No NVM prog or erase routine can be called until this NVM operation is completed.

6.3.13 NVMCLKFAC setting routine

This routine is used to write the NVMCLKFAC Bit in SYSCON0 register.

Table 6-27 NVMCLKFAC setting subroutine

Subroutine	**00003855_H: USER_NVMCLKFAC_SET** Prototype: void **USER_NVMCLKFAC_SET**(char Value)
Input	**Value (char)**: SYSCON0.NVMCLKFAC value to be written. b
Output	--

6.3.14 RAM MBIST starting routine

This routine is used to perform a RAM test. A linear write/read algorithm using alternating data is executed on a RAM range specified by the start and stop addresses given as input parameters. When starting the MBIST test, standard RAM interface is disabled.

Therefore data stored into it will not be accessible and data stored in the memory range under test will be cleared to zero. The standard interface will be re-enabled after completion before the end of the routine execution.

Note: The start and stop address passed as parameter are offsets to be added to the RAM start address (18000000_H*).*

Table 6-28 RAM MBIST start subroutine

Subroutine	**$0000384D_H$: USER_RAM_MBIST_START** Prototype: char **USER_RAM_MBIST_START**(unsigned short RAM_MBIST_Stop_Addr, unsigned short RAM_MBIST_Start_addr)
Input	**RAM_MBIST_Stop_Addr (unsigned short):** RAM offset of the stop address of RAM range to be tested **RAM_MBIST_Start_addr (unsigned short):** RAM offset of the start address of RAM range to be tested
Output	**Returned value (char): Pass or Fail** Bit 0: MBIST pass or fail 0 = MBIST test pass 1 = MBIST test fail Bit 1: Address range fail 0 = test routine pass (address range valid) 1 = test routine fail (address range invalid) Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed 1 = Fail: Routine was not executed Possible reason for execution fail: - Routine called as nested during the execution of another NVM routine (e.g. via RAM branching)

Note: While test is running, no RAM access should be attempted on the whole RAM.

6.3.15 NVM ECC check routines

The firmware provides 2 different routines to enable the user to check and monitor the quality of the NVM cells upon shipment and/or over the lifetime of the device.

The first routine, USER_NVM_ECC_CHECK, provides an easy way for the user to perform a quick check of the status of the whole NVM array. The routine performs a read of the complete NVM returning the single and double bit ECC flags. This is meant to be

used as a quick check of the programming quality of the NVM Code region and the mapped pages of the NVM Data region.

Table 6-29 NVM ECC check subroutine

Subroutine	**00003845_H: USER_NVM_ECC_CHECK** Prototype: char **USER_NVM_ECC_CHECK**(void)
Input	--
Output	**Returned value (char): ECC error indication** Bit 0: ECC1READ 0 = No single bit ECC error on the whole NVM read. 1 = At least one single bit ECC error on the whole NVM read Bit 1: ECC2READ 0 = No double bit ECC error on the whole NVM read. 1 = At least one double bit ECC error on the whole NVM read Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via test is running, no RAM access should be attempted on the whole RAM. branching)

Note: The USER_NVM_ECC_CHECK routine performs a read of the entire NVM code region and of all the non-erased (mapped) pages of the Data region. All logical pages of the Data NVM region not yet programmed and consequently not mapped) are not checked since there is no link to a physical address. In case the user needs to completely check the NVM Data region, a program of all the logical pages of the sector has to be performed before calling the USER_NVM_ECC_CHECK

The second routine, USER_ECC_CHECK, provides a way to check whether during code execution any ECC error occurred. With its return value the routine indicates if a single or a double bit error ECC error flag was set since last power-off (incl. Sleep Mode) of the device, last call of this routine or since last call of a user routine for NVM operation, whatever happened last. This routine is meant to be used over device life time to monitor the occurrence of ECC errors. In addition, in case of EEC2 error, the routine will provide as an output the address of the last ECC2 error occurred.

The address is reported as an output in the RAM location passed as a pointer. The returned value always provides the starting address of the 8 Byte section where the ECC error happened.

Table 6-30 ECC check subroutine

Subroutine	**0000383D$_H$: USER_ECC_CHECK** Prototype: char **USER_ECC_CHECK**(unsigned int * ECC2Addr)
Input	**ECC2Addr (unsigned int pointer):** Pointer to the RAM location where the last NVM address with ECC2 error shall be stored
Output	**Returned value (char): ECC error indication** Bit 0: ECC1READ 0 = No single bit ECC error on the whole NVM read. 1 = At least one single bit ECC error on the whole NVM read Bit 1: ECC2READ 0 = No double bit ECC error on the whole NVM read. 1 = At least one double bit ECC error on the whole NVM read Bit 7: Execution Pass/Fail status 0 = Pass: Routine was correctly executed. 1 = Fail: Routine was not executed Possible reason for execution fail: - Routine called as nested call during the execution of another NVM routine (e.g. via test is running, no RAM access should be attempted on the whole RAM. branching)

Note: The ECC error flags, provided as output of the NVM ECC check routines, are a copy of the ECC internal error flags registers. These registers are set when a read access to the NVM results in a single and/or double bit error and are cleared only in case of power-off (incl. Sleep Mode) or in the following cases:

1. *When programming or erasing a NVM page.*
2. *When calling the USER_NVM_ECC_CHECK routine before performing the NVM complete read.*
3. *When calling the USER ECC check routine before returning to user code.*

6.3.16 NVM protection status change routines

These routines allow to enable or disable the read or write protection individually on the NVM Code Sectors (Linearly mapped NVM sectors) and on the NVM Data Sectors (Not linearly mapped NVM sectors).

These routines control the protection status updating the value of the lower nibble of the NVM_PROT_STS register. The status of the register will be anyhow restored according

to the NVM PASSWORD stored in the Configuration Sector at next reset. Please, refer to User Manual for NVM_PROT_STS bits description.

*Note: Each routine requires a password (16 bit) that shall be provided as an input to the user routine call. The BootROM code will compare this password with the one stored into the configuration sector 100TP page 1 (offset $0C_H$ for the routines addressing the linearly mapped region protection and offset $0E_H$ for the routines addressing the non linearly mapped region protection). Only in case the password read out of the 100TP page 1 matches the password provided as input, the requested protection status change is performed (refer to **Table 6-11**).*

Table 6-31 NVM Code sectors (linearly mapped NVM sectors) write protection enable subroutine

Subroutine	**00003925_H: USER_CFLASH_WR_PROT_EN** Prototype: bool **USER_CFLASH_WR_PROT_EN**(unsigned short CFLASH_PW)
Input	**CFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0C_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(1) to 0.

Table 6-32 NVM Code sectors (linearly mapped NVM sectors) write protection disable subroutine

Subroutine	**$0000391D_H$: USER_CFLASH_WR_PROT_DIS** Prototype: bool **USER_CFLASH_WR_PROT_DIS**(unsigned short CFLASH_PW)
Input	**CFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0C_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(1) to 1.

Table 6-33 NVM Code sectors (linearly mapped NVM sectors) read protection enable subroutine

Subroutine	**00003915_H: USER_CFLASH_RD_PROT_EN** Prototype: bool **USER_CFLASH_RD_PROT_EN**(unsigned short CFLASH_PW)
Input	**CFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0C_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(3) to 0.

Table 6-34 NVM Code sectors (linearly mapped NVM sectors) read protection disable subroutine

Subroutine	**$0000390D_H$: USER_CFLASH_RD_PROT_DIS** Prototype: bool **USER_CFLASH_RD_PROT_DIS**(unsigned short CFLASH_PW)
Input	**CFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0C_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(3) to 1.

Table 6-35 NVM Data sectors (not linearly mapped NVM sectors) write protection enable subroutine

Subroutine	**00003905_H: USER_DFLASH_WR_PROT_EN** Prototype: bool **USER_DFLASH_WR_PROT_EN**(unsigned short DFLASH_PW)
Input	**DFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0E_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(0) to 0.

Table 6-36 NVM Data sectors (not linearly mapped NVM sectors) write protection disable subroutine

Subroutine	**$000038FD_H$: USER_DFLASH_WR_PROT_DIS** Prototype: bool **USER_DFLASH_WR_PROT_DIS**(unsigned short DFLASH_PW)
Input	**DFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset $0E_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(0) to 1.

Table 6-37 NVM Data sectors (not linearly mapped NVM sectors) read protection enable subroutine

Subroutine	**000038F5$_H$: USER_DFLASH_RD_PROT_EN** Prototype: bool **USER_DFLASH_RD_PROT_EN**(unsigned short DFLASH_PW)
Input	**DFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset 0E$_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(2) to 0.

Table 6-38 NVM Data sectors (not linearly mapped NVM sectors) read protection disable subroutine

Subroutine	**000038ED$_H$: USER_DFLASH_RD_PROT_DIS** Prototype: bool **USER_DFLASH_RD_PROT_DIS**(unsigned short DFLASH_PW)
Input	**DFLASH_PW(unsigned short)**: Password to be compared to the one stored in the 100TP page 1 (offset 0E$_H$)
Output	**Returned value (bool): Pass or Fail** 0 = Operation completed successfully. 1 = Operation failed. (Password does not match)

This routine sets the bit NVM_PROT_STS(2) to 1.

For the NVM protection mechanism, user configuration sector pages (100TP) are considered being part of the NVM code area.

Read protection does not block code fetching.

Note: Copying code from NVM to RAM requires a normal NVM read execution and so is blocked in case NVM Read Protection is enabled.

Read protection is meant to protect user application code from hacking. Hence, even if read protection is enabled on Code region, Data regions or both, the code executed from

Code NVM region can always read both NVM Code and Data regions. Please, refer to the User Manual for more information about read and write protection mechanism.

6.4 NVM user applications

The NVM user routines application is described in this section.

6.4.1 NVM Data sector handling

The NVM provides a special sector for Data storage. Through a non-linear mapping of the address space, the FW and the NVM module provides a special feature to increase the maximum number of write-erase cycles a logical page can stand and to reduce the risk of data loss in case of interrupted NVM operations (tearing events).

The handling of this special Data sector requires the usage of an NVM internal look-up table (MapRAM) which is used to store and handle the link between logical and physical addresses of the sector's pages.

Since the MapRAM is a volatile memory, the firmware takes care to rebuild the MapRAM content at each power up based on mapping information stored into a specific field of the Data sectors pages (mapblock). This process is called Data sector initialization (MapRAM initialization).

During this initialization phase, mapping errors induced by tearing events might be found. This would then prevent the firmware from properly restoring the link between the logical and physical addresses thus preventing proper usage of this sector. In this case, the firmware provides a specific algorithm (Service Algorithm) to identify and solve these errors. In particular, the Service Algorithm tries to repair bad pages created unintentionally into the NVM Data region due to, for example, a NVM program or erase operation interrupted by any reset or power loss (tearing events). The Service Algorithm is triggered during the startup by the NVM data sector initialization in case mapping issues are found.

The Service Algorithm provides proper analysis features to try to preserve the integrity of the NVM Data region in case ongoing NVM operation (program or erase) is unintentionally and unexpectedly aborted (e.g. due to power loss). Anyhow, it is not meant to cover all possible scenarios that can be created by an interrupted NVM operation. The user shall put in place proper action to avoid any possible interruption of NVM operation (e.g. using proper capacitor on the power supply).

The NVM data sector initialization and Service Algorithm flows are described below.

NVM Data sector initialization

Upon power on reset, brown out reset, pin reset, WDT1 reset or wake up from sleep reset, as part of the start up, the firmware triggers a NVM initialization of the NVM data

sector. This initialization is performed by a hardware state machine which takes care to restore the mapping information into the MapRAM reading specific bytes (called mapblock) of the NVM data sector pages (see **Figure 6-3**). The state machine accesses these bytes and, page by page, reads out the logical page to which the current physical page has to be linked to, updating accordingly the dedicated MapRAM location.

In case a mapblock is read as erased, the physical page is not mapped. All the logical pages for which no valid mapping is found are marked into the MapRAM as unmapped.

While reading out the info from the mapblock, the hardware state machine might find incorrect mapping info. In particular, following scenarios might appear:

- more physical pages are mapped to the same logical page (double or higher mapping)
- the mapblock information cannot be read correctly due to ECC errors (faulty page)

In this case, the hardware state machine stops the initialization on the first incorrect mapping and triggers the execution of the Service Algorithm (SA).

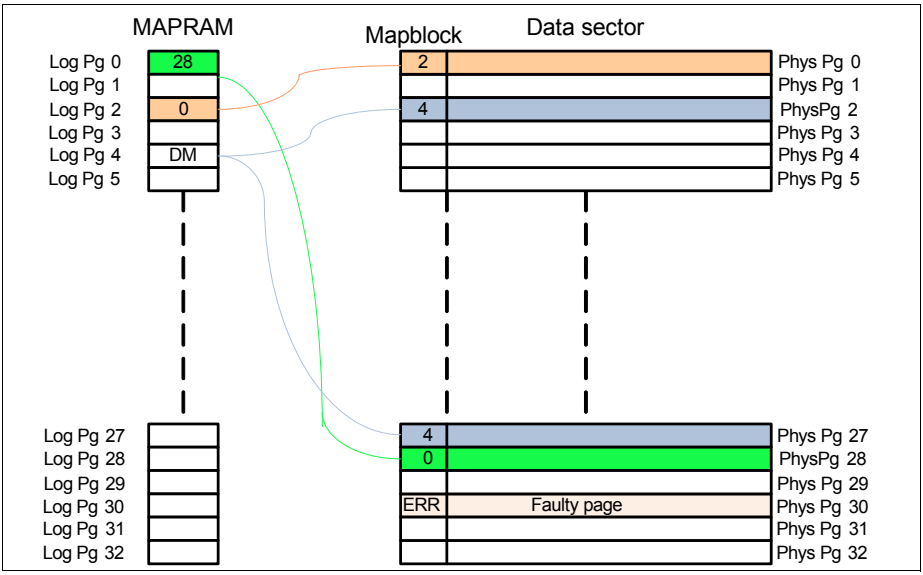

Figure 6-3 MapRAM and Mapblocks

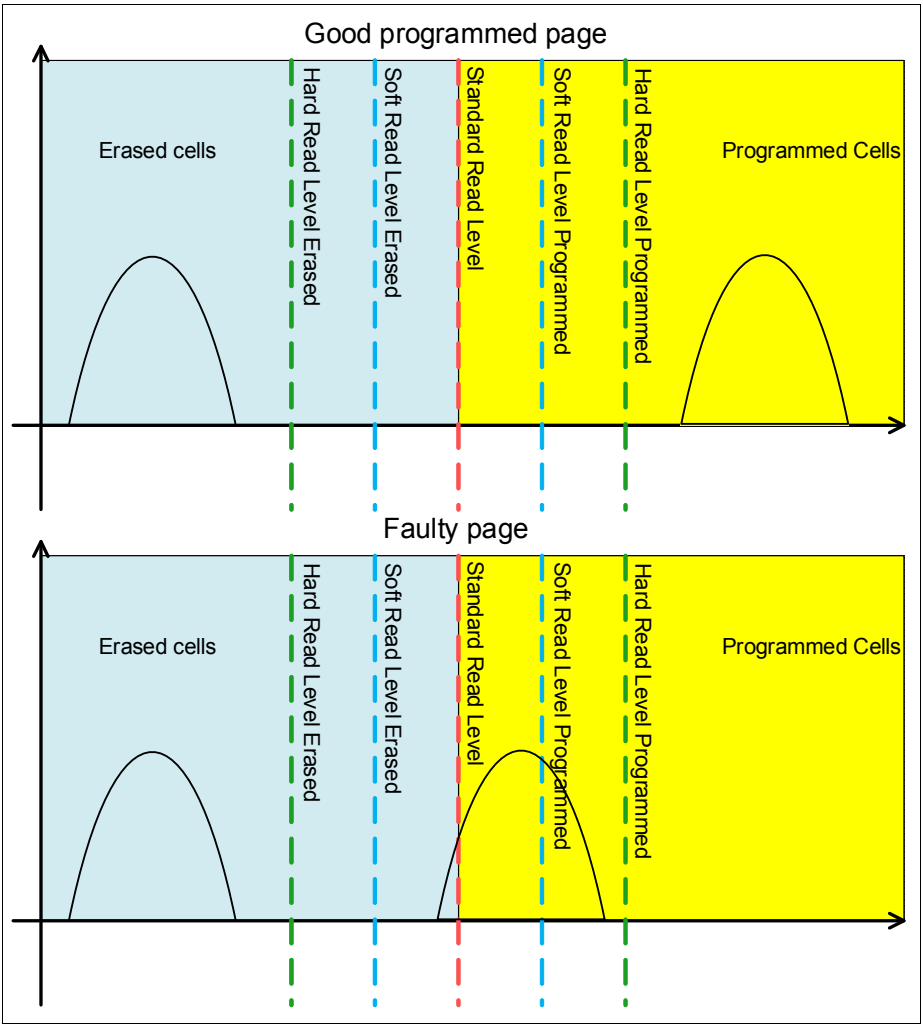

Figure 6-4 Read levels and faulty page

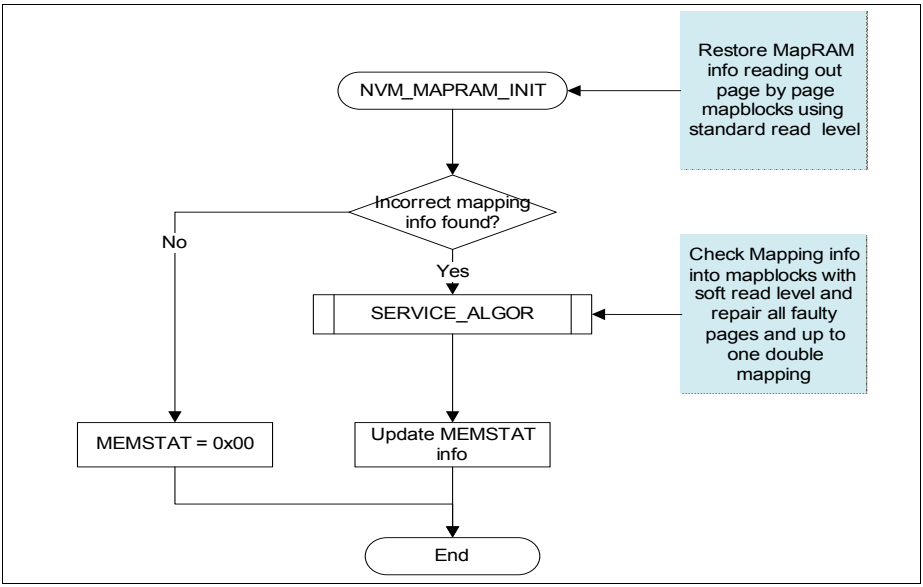

Figure 6-5 NVM data sector initialization flow

In order to detect pages whose mapblock is marginal towards the standard read level, the NVM finite state machine that performs the mapping initialization is triggered three times with three different read levels: standard read margin, soft read level erased and soft read level programmed (refer to **Figure 6-4**). As soon as the first incorrect mapping (faulty or multiple mapping) is detected by any of these three initialization sequences the Service Algorithm is called.

At the end of the Service Algorithm execution, a new initialization of the Data sector is needed to properly initialize the mapping info. This final initialization is again executed by triggering the NVM Finite State Machine and is performed using only the standard read level.

Note: The result of the last NVM Data sector initialization executed during the startup flow is reported to the user via the bit 1 of the SYS_STRTUP_STS register (MRMINITSTS). If this bit is set to 1 then the last initialization failed and the mapping info might be corrupted. In this case, a reset (power on reset, brown out reset, pin reset or wakeup reset) can be issued in order to start the Service Algorithm to try to fix the integrity issue inside the Data NVM. If the MRAMINITSTS is still flagged afterwards, the Data NVM sector has to be re-initialized by performing a sector erase.

Service Algorithm

The Service Algorithm is called by the NVM Data sector initialization in case incorrect mapping issues have been found. The Service Algorithm checks the data sector page by page reading the mapblocks with soft read levels (refer to **Figure 6-4**).

At first, the Service Algorithm looks for faulty pages and tries to repair them by erasing these pages. Following, the algorithm proceeds looking for double or higher mappings.

In case two or more double mappings or at least one triple or higher mapping were found the SA stops execution and reports an error on the MEMSTAT register (MEMSTAT set to $A0_H$). In case, instead only one double mapping is found, the algorithm selects which page has to be erased according to the following steps:

1. The SA checks the 2 pages linked to the double mapping with standard, soft and hard read levels to detect which one has better quality (more margin towards the standard read level, refer to **Figure 6-4**). The page with smaller margin is then erased.
2. In case both pages have same quality, the algorithm checks some specific bits of the mapblock (called map counter) to check which of the pages has been programmed last. In this case, the older one is erased.

In case both pages have same map counter value, the SA cannot decide which page has to be erased and ends the flow reporting an error on the MEMSTAT register (MEMSTAT set to $A0_H$).

Whenever the SA is triggered, the addressed data sector number will be stored in SECTORINFO (this is an indication that the SA was executed during the start up phase). In addition, in case the SA cannot recover all incorrect mapped pages, the SA reports a fail into the SASTATUS field of the MEMSTAT writing the value 10_B. In such a case, the user shall properly handle the reported mapping issue by either triggering a reset (Power on reset, pin reset, WDT1 reset, brown out reset or wake up from sleep reset) in order to trigger a new NVM initialisation or to erase the whole NVM data sector to reset the mapping info.

Detailed description of the MEMSTAT register can be found in the following table **Table 6-39**.

Table 6-39 MEMSTAT Register Status for NVM Integrity Handling

Field	Bits	Description
SASTATUS	7:6	**Service Algorithm Status** 00 Depending on SECTORINFO, 2 possible outcomes. For SECTORINFO = 00_H: NVM initialisation successful, no SA is executed. For SECTORINFO = Otherwise: SA execution successful. Only 1 mapping error fixed. 01 SA execution successful. At least 1 mapping error fixed. 10 SA execution failed. Map error in data sector. 11 Reserved
SECTORINFO	5:0	**Sector Information** 01_H to 20_H representing the different sector addresses. For values not within this range, the data will be considered invalid. Once the SA has been executed, regardless of the execution status, the last access sector information will be stored here.

Note: The MEMSTAT register has a dual function. It is used to store the return value of the SA as well as input value for the NVM operations to indicate the Emergency Operation. For this reason, the user shall reset the MEMSTAT register after every power on reset, brown out reset, pin reset or wake up reset before the execution of any NVM operation.

During the repair phase, pages with incorrect mapping are erased. Each page erase operation takes up to 4.5 ms.

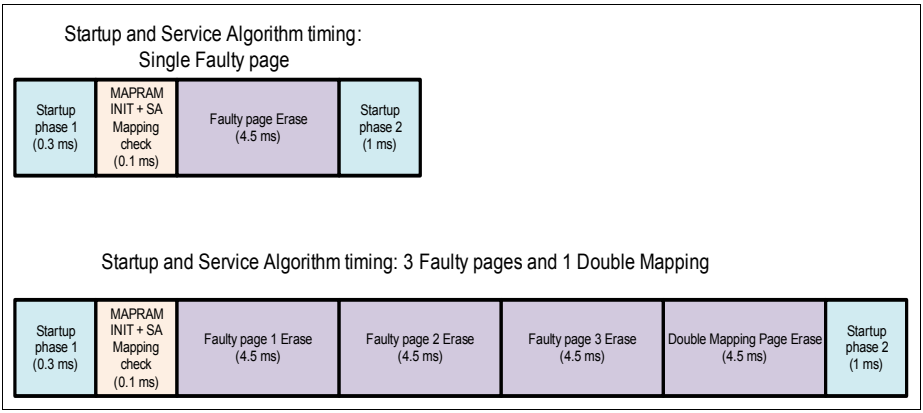

Figure 6-6 Service Algorithm: Timing examples

Due to the duration of the first WDT1 open window after reset (long open window), the maximum number of pages that can be repaired in one Service Algorithm execution is 13.

The result of the Service Algorithm repair phase is reported in the MEMSTAT register. At the end of the startup procedure, user **shall** evaluate the content of this register to properly handle fails and clear the register before performing any NVM operation.

The value is only available after reset before any NVM operation (Program, Erase, OpenAB) is started. The corresponding NVM address to the Sector Information read is listed in **Table 6-3**.

Service Algorithm and NVM Protection

In case the Service Algorithm detects mapping issues, it tries to repair mapping by erasing the wrong pages (either faulty or double mapped pages). Consequently, the repair step can modify the NVM Data sector content. To avoid data loss, the SA checks the NVM data sector protection and proceeds towards the repair step only if the protection is not enabled.

In case protection is enabled, instead, the repair actions are not performed and a warning is provided to the user by writing the value FE_H in the MEMSTAT register.

Via a dedicated 100TP sector parameter the user can always allow Service Algorithm to perform the repair step even in case the Data sector is protected. The control Byte for this feature, CS_SA_WITH_PROT_EN, is stored into the first 100TP page (refer to **Table 6-11**). When this parameter is set to the value $A5_H$ the repair step is executed even in case protection is set. The repair flow saves the protection setting, removes temporarily the protection on the data sector, performs the needed repair operation and

then restores the original protection settings. The temporary protection disabling is performed at NVM protection register, no access or changes to the user defined NVM protection password is performed. By default the CS_SA_WITH_PROT_EN parameter is set to 00_H (i.e. protection status is considered).

6.4.2 Supporting Background NVM Operation

There is only one NVM module present in TLE986xQX. When NVM is busy executing internal operations (e.g. cells programming or erasing, data verify), no other activities within NVM can be executed. Although the NVM programming or erasing is handled by the NVM module, the user code cannot be read or executed as the NVM module is busy.

For this reason interrupts can only be serviced when the NVM is free if the interrupt vector table or interrupt service routines are located in the NVM. A NVM program operation can take from 500 us to 13.5 ms to be completed. Therefore there is a need to support the user for critical activities.

To support other user activities while NVM is busy, the BootROM can redirect code execution to RAM after triggering time consuming NVM operations like program and erase. This type of background code execution is known as Type 2 NVM operations or RAM branching. When RAM branching is active, the BootROM routines jump to the RAM address 18000400_H every time it has to wait for NVM internal operation to be completed. In this way, the user can execute code from RAM while NVM is busy.

While executing user code from RAM due to RAM branching, if the ongoing internal NVM operation is completed, the BootROM code execution is not automatically restarted and the previously triggered BootROM user routine is suspended. The user needs to explicitly re-trigger the user routine code execution by giving back control to the BootROM via a return instruction (BX LR). In this way the suspended user routine execution is resumed.

The USER_NVMRDY user routine (refer to **Chapter 6.3.5**) is provided to check whether the internal on going NVM operation is finished. User can use this routine to poll the busy status of the NVM to decide when to return control to the suspended user routine.

In case the user RAM code returns control to BootROM user routine while NMV is still busy, the BootROM code waits till the internal operation is completed before continuing with the normal user routine execution.

Table 6-40 shows RAM branching address and provides an example for the RAM code exit point. **Figure 6-7** shows how background programming can be supported during calls to a NVM programming routine.

Note: The context switch between BootROM user routine and user RAM code in NVM operation Type 2 is user responsibility. To avoid that RAM code execution interferes with BootROM user code completion, the user must save the content of the used resources (e.g. core registers) upon starting

the RAM code execution and restore them before jumping back to the BootROM code. Under no circumstances shall the user return with modified core registers, as proper resuming the BootROM function cannot be ensured.

Note: During user RAM code execution in Type 2 NVM operations, no calls to NVM user routine are allowed. Calling other NVM user routines can change internal NVM registers content thus affecting the completion of the suspended operation.

Table 6-40 RAM branch code structure

RAM Address	RAM content
18000400_H	Start of user defined code. It can be directly code or jump to some other RAM location
End of user defined code location	BX LR (Return instruction)

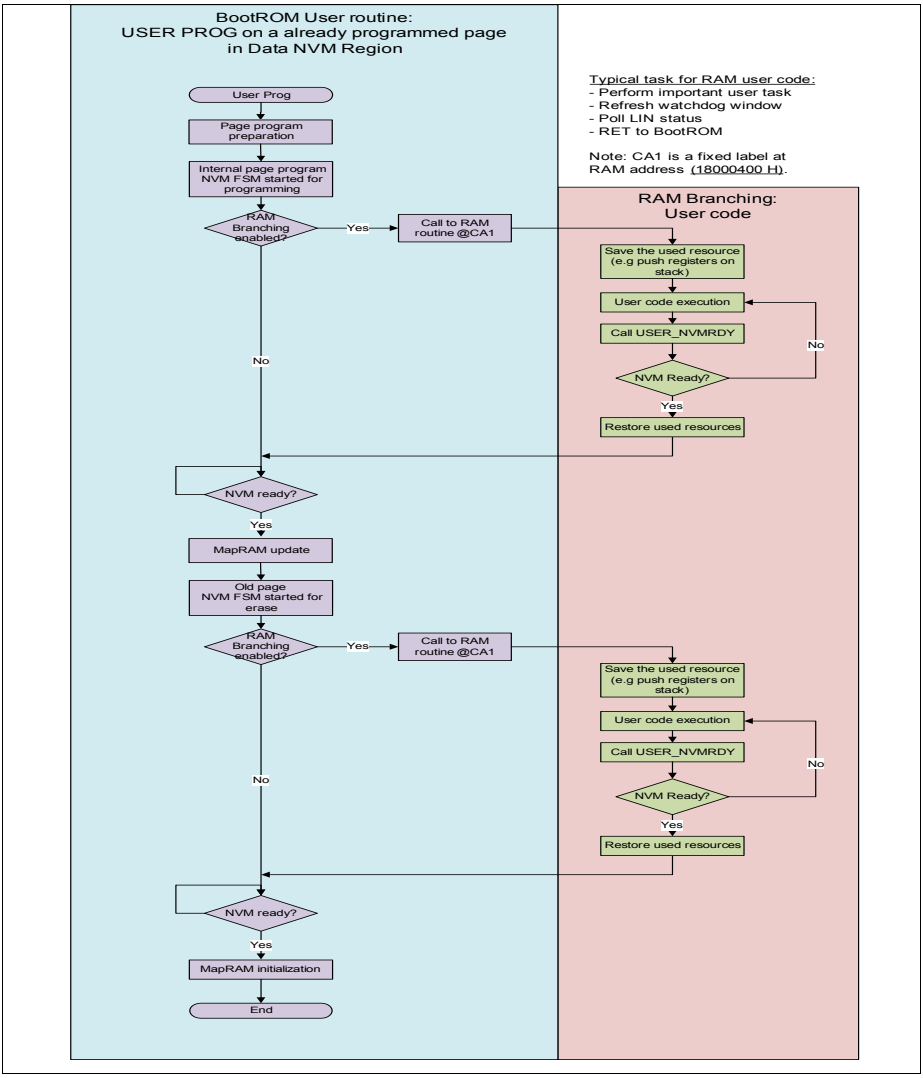

Figure 6-7 Background NVM programming operation with jumps to RAM code (example for non-linearly mapped sector)

6.4.3 Emergency operation handling

Note: Emergency operation provides the possibility to exit an on-going NVM operation in a faster way skipping some internal time consuming steps in case high priority tasks are required. For this reason, leaving an NVM operation via an emergency operation request might leave some inconsistent data into the sector targeted by the interrupted operation. When using this feature on Data NVM sector, the user is recommended, soon after the completion of the execution of the high priority tasks, to issue a pin reset or sleep entry-exit sequence to let the firmware to properly clean the sector.

To ensure that NVM is functioning correctly, all NVM operations (i.e. program or erase) are to be completed before a new NVM operation is started. In addition, corrective activities such as retries and disturb handling are added in an NVM program routine and could add additional time. In an emergency situation, where the system needs to save important user data in the shortest time possible, this becomes critical. Therefore, a mechanism to bypass these corrective activities as well as to inform that a new NVM sequence will not be started, is needed. To support an emergency situation, the following steps are recommended in the code whenever the NVM programming is called.

6.4.3.1 Emergency operation handling - Type 1 routines

For Type 1 routines (including both program and erase), an emergency programming may only be handled with the interrupt enabled shown in **Table 6-41**.

Table 6-41 Emergency operation handling in Type 1 routines

Step	Description
1	User code enables interrupt and sets MEMSTAT.NVMPROP before calling NVM (Program/Erase) routines.
2	While the NVM operation is on-going, an event occurs triggering an interrupt.
3	Interrupt subroutine (ISR) is serviced immediately when the NVM is free.
4	ISR has to check for the MEMSTAT.NVMPROP status. If this Bit is set, MEMSTAT.EMPROP has to be set and ISR has to be exited.
5	With control returned to the BootROM, the NVM routines will be executed bypassing the corrective activities. This ensures that the routines are completed in the shortest time possible
6	Exiting the NVM routines, the user code checks the MEMSTAT.EMPROP. Since it is set, the code can branch to execute a user defined emergency sequence and clear the Bits MEMSTAT.NVMPROP and MEMSTAT.EMPROP. These activities can include the programming of the critical data.

6.4.3.2 Emergency operation handling - Type 2 routines

For Type 2 routines (including both program and erase), an emergency programming may be handled with or without the interrupt enabled. In the case with interrupt enabled, it is similar to Type 1 Routines shown in **Table 6-41**. For the case without interrupt enabled, it is shown in **Table 6-42**.

Table 6-42 Emergency operation handling in Type 2 routines (No interrupt)

Step	Description
1	User code sets MEMSTAT.NVMPROP before calling NVM (Program/Erase) routines.
2	While the NVM operation is started, the BootROM jumps to execute a user defined code in the RAM. Within this code, the user checks periodically for critical events.
3	During the checking, an emergency event occurs. The code has to set MEMSTAT.EMPROP and give back control to BootROM.
4	With control returned to the BootROM, the NVM routines will be executed bypassing the corrective activities. This ensures that the routines are completed in the shortest time possible
5	Exiting the NVM routines, the user code checks the MEMSTAT.EMPROP. Since it is set, the code can branch to execute a user defined emergency sequence and clear the Bits MEMSTAT.NVMPROP and MEMSTAT.EMPROP. These activities can include the programming of the critical data.

6.4.3.3 Emergency operation handling timing

In this chapter some information about overall emergency operation worst case timing is provided.
Table 6-43 describes the case in which user data has to be saved into the linear sector due to an emergency event. Flow for programming the critical information in the not linearly mapped region of the NVM is similar (step 6 and 7 are inverted and a few µs have to be added for MapRAM update) and overall worst case time is the same.

Table 6-43 Emergency operation handling in Type 1 routines

Phase	Description
1	User code enables interrupt and sets MEMSTAT.NVMPROP before calling NVM (Program/Erase) routines.
2	While the NVM operation is on-going, an event occurs triggering an interrupt. In the worst case interrupt comes soon after a new erase was started.

Table 6-43 Emergency operation handling in Type 1 routines (cont'd)

Phase	Description
3	Interrupt subroutine (ISR) is serviced immediately when the NVM is free.
4	With control returned to the BootROM, the NVM routines will be executed bypassing the corrective activities. This ensures that the routines will end in the shortest time possible even if a successful execution of the on going NVM operation is not ensured.
5	Exiting the NVM routines, the user code checks the MEMSTAT.EMPROP. Since it is set, the code can branch to execute a user defined emergency sequence. First step is open AB and load user relevant data.
6	Before programming new data, if target page is already used, a preliminary erase is performed.
7	User critical data are programmed in the target page.

The **Table 6-43** refers to the type 1 routines but data are similar for type 2 routines as well.

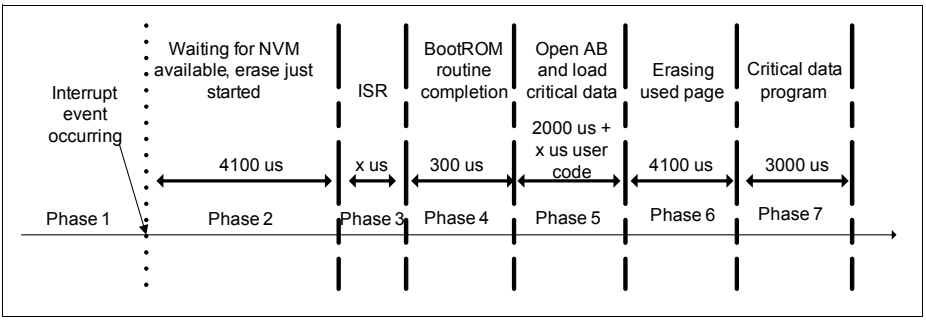

Figure 6-8 Worst case emergency handling timing when linear sector is used

Worst case time, shown in **Figure 6-8**, is then 13.5 ms. This does not include time for user code execution. It can be reduced by about 4.1 ms if the user ensures that the page used for critical data saving is erased.

6.4.4 NVM user routines operation

This section describes the application of some NVM user routines.

6.4.4.1 NVM user programming operation

In TLE986xQX, the NVM supports programming of up to 128 Bytes of data at once. The user can execute the following sequence illustrated in **Figure 6-9** for NVM user

programming. Once the assembly buffer has been successfully opened, the user can load the assembly buffer with the user defined contents. This can be achieved by a store instruction targeting the selected byte in the NVM page opened with the OPEN_AB user routine.

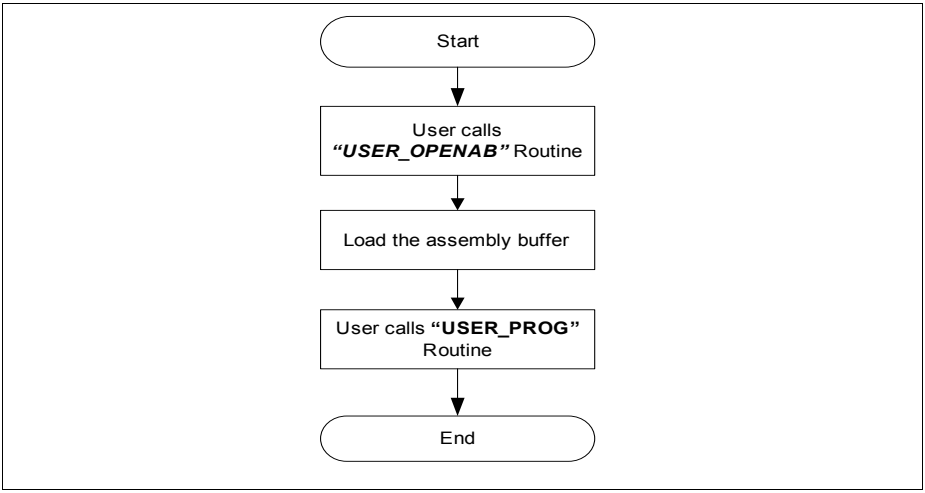

Figure 6-9 NVM user program

6.4.4.2 Tearing-safe Programming

In TLE986xQX, the mapping mechanism of the non-linearly mapped sector is used like a log-structured file system. When a page is programmed in this sector, the old values are not physically overwritten, but a different physical page (spare page) in the same sector is programmed. If the programming fails, the old values are still present in the sector and user can decide, by means of a specific input parameter of the user programming routine (refer to **Table 6-16**), whether the old values or the new failing values should be physically kept in the sector.

When an erase or write procedure is interrupted by a power down, this is identified during the reconstruction of the MapRAM content after the next reset. In this case, the service algorithm routine is automatically started and repairs the NVM state exploiting the fact that either the old or the new data (or both) are fully valid

6.4.4.3 NVM user erase operation

The user can execute the following sequence illustrated in **Figure 6-10** for NVM user erase.

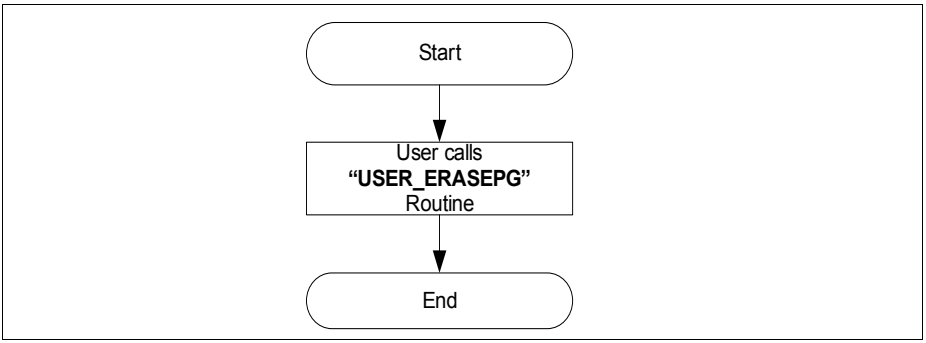

Figure 6-10 NVM user erase

6.4.4.4 NVM user programming abort operation

The user can execute the following sequence illustrated in **Figure 6-11** for NVM user programming abort.

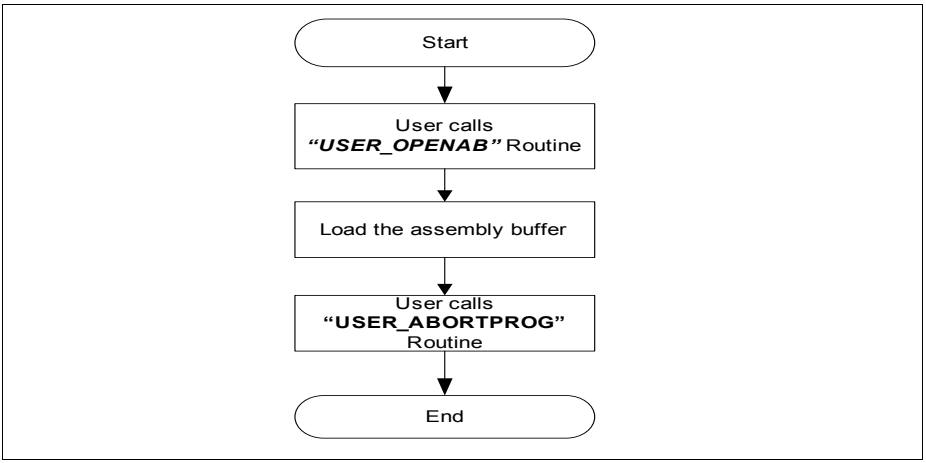

Figure 6-11 NVM user abort program

6.4.5 NVM protection mechanism

User can use BSL mode 6 of LIN, FAST LIN or UART to control the NVM protection by providing or deleting a dedicated password. (please refer to **Section 4.4.4.5** and **Section 5.2.2.7** for more details regarding NVM password setting). Once a valid password (different from 00000000_H and $FFFFFFFF_H$) is programmed, program and read protection on both code and data NVM regions is enabled upon startup regardless

of reset source. During normal operation, if user wishes to program or read the NVM memories, he can temporarily disable the NVM protection writing the desired protection settings into the least significant nibble of the NVM_PROT_STS register by means of the dedicated BootROM functions (refer to **Section 6.3.16**)

TLE986xQX BE- Step

Revision History:	**2015-07-10**	Rev. 1.3
Previous Version:	First Version	

Page	Subjects (major changes since last revision)

Edition 2015-07-10

Published by
Infineon Technologies AG
81726 München, Germany

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