UM2035
User manual

Evaluation board with STM32F769NI MCU

Introduction

The STM32F769I-EVAL evaluation board is a complete demonstration and development platform for STMicroelectronics ARM® Cortex®-M7 core-based STM32F769NI microcontrollers. It features the following interfaces: four I²Cs, six SPIs with three multiplexed full-duplex I²S, SDIO, two SAIs, 8-bit to 14-bit digital camera, Ethernet MAC, FMC, Quad-SPI. It also features four USARTs and four UART peripherals, two CAN buses, three 12-bit ADC converters, two 12-bit DAC channels, internal 512 Kbytes of SRAM + 16 Kbytes of instruction, 2 Mbytes of Flash memory, TCM RAM + 4 Kbytes of backup SRAM, USB OTG HS and USB OTG FS peripherals, SWD and JTAG debugging support. This evaluation board can be used as a reference design for user application development but it is not considered as a final application.

The full range of hardware features on the board helps the user to evaluate all the peripherals (USB OTG HS, USB OTG FS, Ethernet, motor control, microSD™ card, USART, audio DAC and ADC, digital microphone, CAN, SRAM, NOR Flash, SDRAM, Quad SPI Flash, 4" DSI LCD with capacitive touch panel etc.) and develop applications. Extension headers make provide an easy mean of connecting a daughterboard for a specific application.The integrated ST-LINK/V2-1 provides an embedded in-circuit debugger and programmer for the STM32.

Figure 1. STM32F769I-EVAL evaluation board

1. Picture is not contractual.

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1 Features

- STM32F769I-EVAL microcontroller with 2 Mbytes of Flash memory, internal 512 Kbytes of SRAM + 16 Kbytes of instruction and TCM RAM + 4 Kbytes of backup SRAM in BGA216 package
- Six options for 5V power supply:
  - Power jack
  - ST-LINK/V2-1 Micro-B USB connector
  - User USB HS connector
  - User USB FS1 connector
  - User USB FS2 connector
  - Daughterboard
- SAI interface audio codec, stereo audio jack which supports headset with microphone
- Two stereo digital microphones, audio jack connector used to connect external speakers
- 4-Gbyte (or more) SDIO interface microSD™ card
- I^2C Extension interface
- RS-232 connector
- JTAG/SWD and ETM trace debug support, ST-LINK/V2-1 embedded
- IEEE-802.3-2002 compliant Ethernet connector
- Camera module
- 8Mx32bit SDRAM, 1Mx16bit SRAM and 8Mx16bit NOR Flash
- 512-Mbit Quad-SPI NOR Flash
- 4" capacitive touch LCD display with MIPI® DSI connector
- Joystick with 4-direction control and selector
- Reset, Wake Up/Tamper or key button
- 4-color user LEDs
- Extension and memory connectors for daughterboard or wrapping board
- USB OTG HS and FS with Micro-AB connectors
- RTC with backup battery
- CAN2.0A/B compliant connector
- Potentiometer
- Motor control connector

2 Demonstration software

Demonstration software is preloaded in the STM32F769NI Flash memory. For more information and to download the latest version, refer to the STM32F769I-EVAL demonstration software available at the *www.st.com* website.

3 Product marking

Evaluation tools marked as "ES" or "E" are not yet qualified and therefore they are not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference design or in production.

"E" or "ES" marking examples of location:

- On the targeted STM32 that is soldered on the board (for illustration of STM32 marking, refer to the section "Package information" of the STM32 datasheet at the *www.st.com* website).
- Next to the evaluation tool ordering part number, that is stuck or silkscreen printed on the board.

4 Ordering information

To order the evaluation board refer to *Table 1*.

Table 1. Ordering information

Order code	Target STM32
STM32F769I-EVAL	STM32F769NI

5 Delivery recommendations

Before using the board for the first time, the user should check that it has not been visibly damaged during the shipment, and that no components are unplugged or missing. When the board is extracted from its plastic bag, check that no component remains in the bag.

The main components to verify are:

1. 25 MHz crystal (X4) which may have been removed by a shock from its socket.
2. The microSD card which may have been ejected from the connector CN17 (right side of the board) and CN30 (bottom side).

Caution: There is a risk of explosion if the battery is replaced by an incorrect one. According to the instructions, make sure to dispose of used batteries.

6 Hardware layout and configuration

STM32F769I-EVAL evaluation board is designed around the STM32F769NI (216-pin in TFBGA package). The hardware block diagram *Figure 2* illustrates the connection between STM32F769NI and peripherals (SDRAM, SRAM, NOR Flash, Quad-SPI Flash, Camera module, color DSI LCD, USB OTG connectors, motor control connector, USART, Ethernet, Audio, CAN, microSD cards and embedded ST-LINK) and *Figure 3* will help the user to locate these features on the evaluation board.The mechanical dimensions of the board are showed in *Figure 4*. The board history version is reported in the yellow frame of the *Figure 25*.

Figure 2. Hardware block diagram

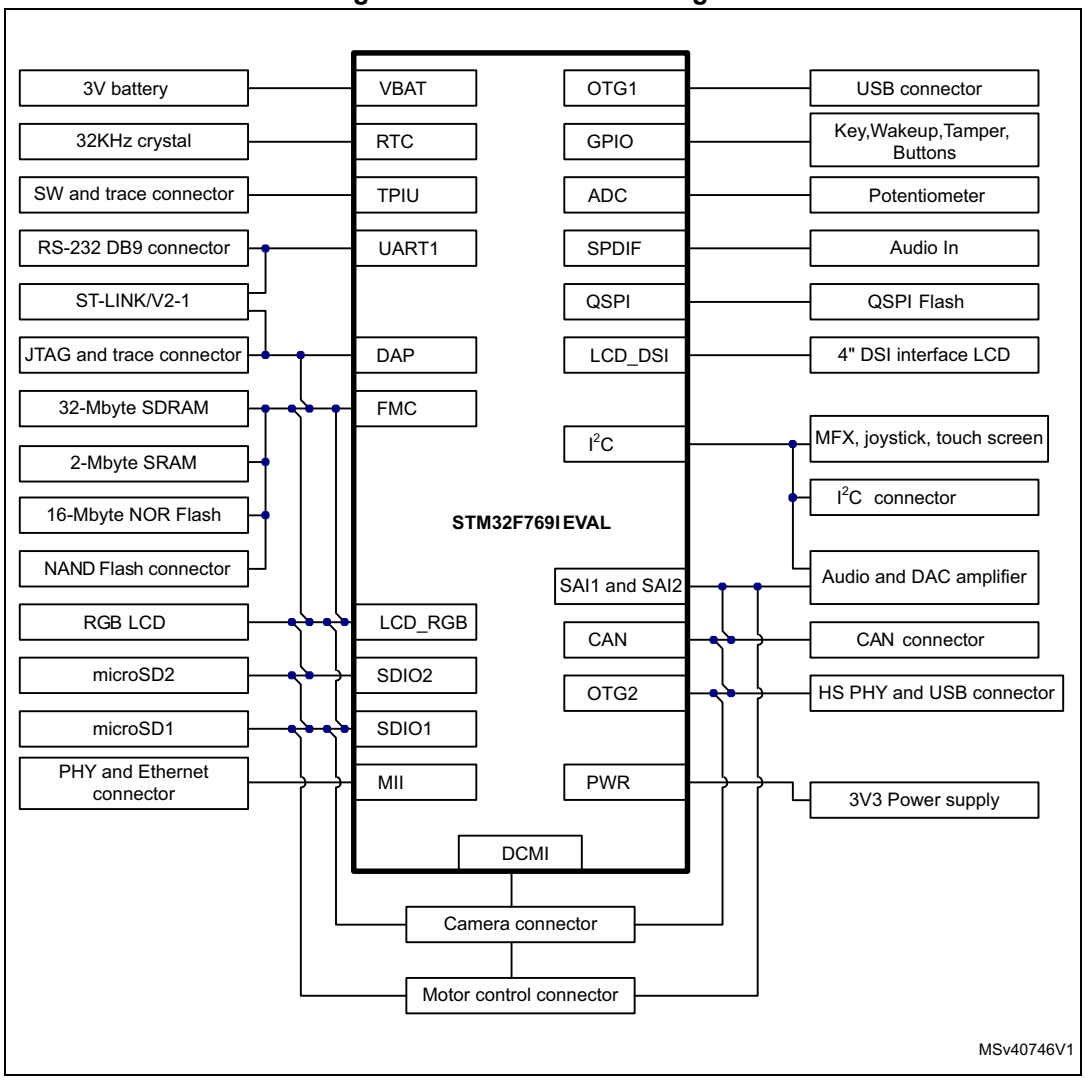


Figure 3. STM32F769I-EVAL evaluation board layout

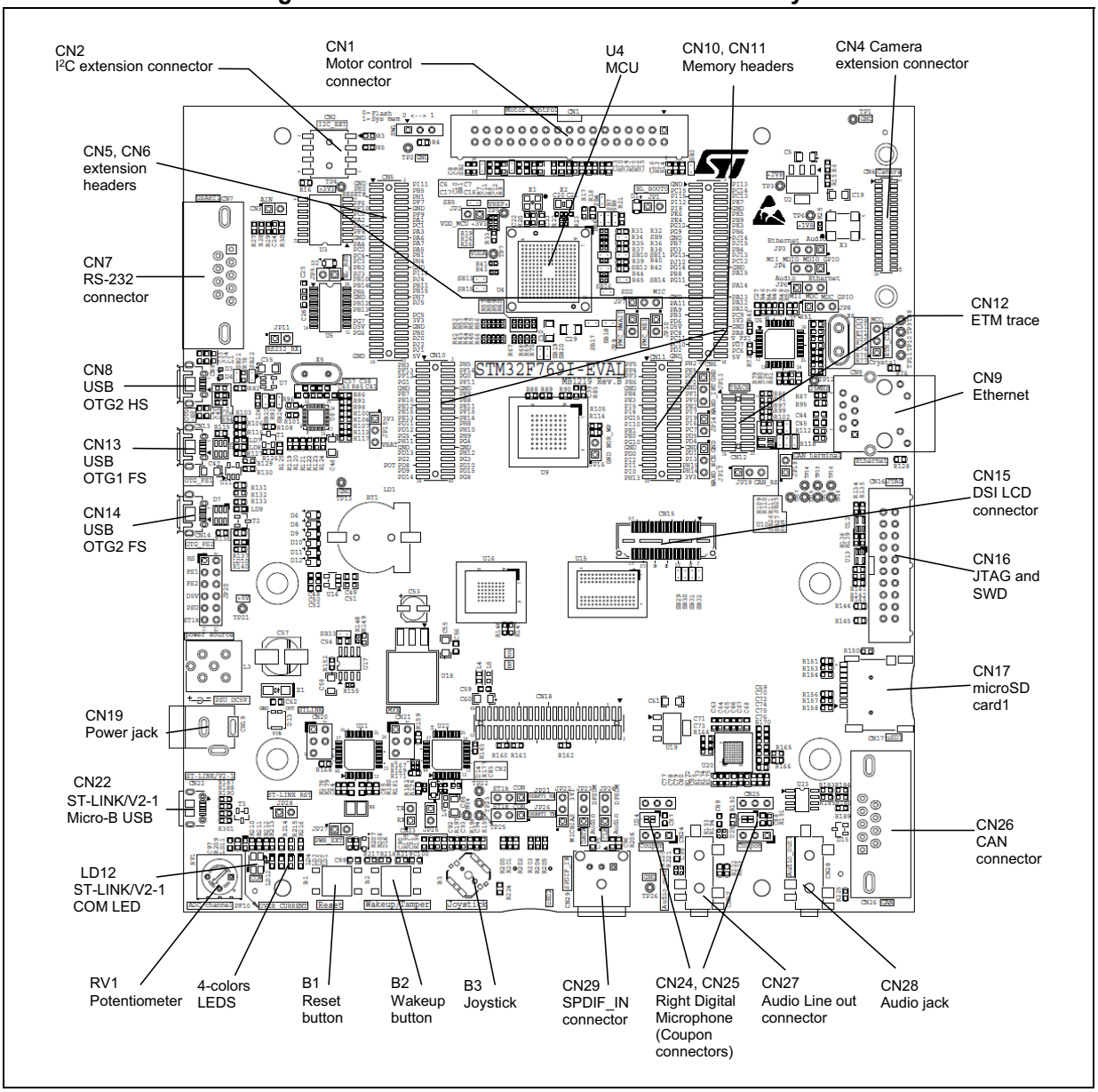
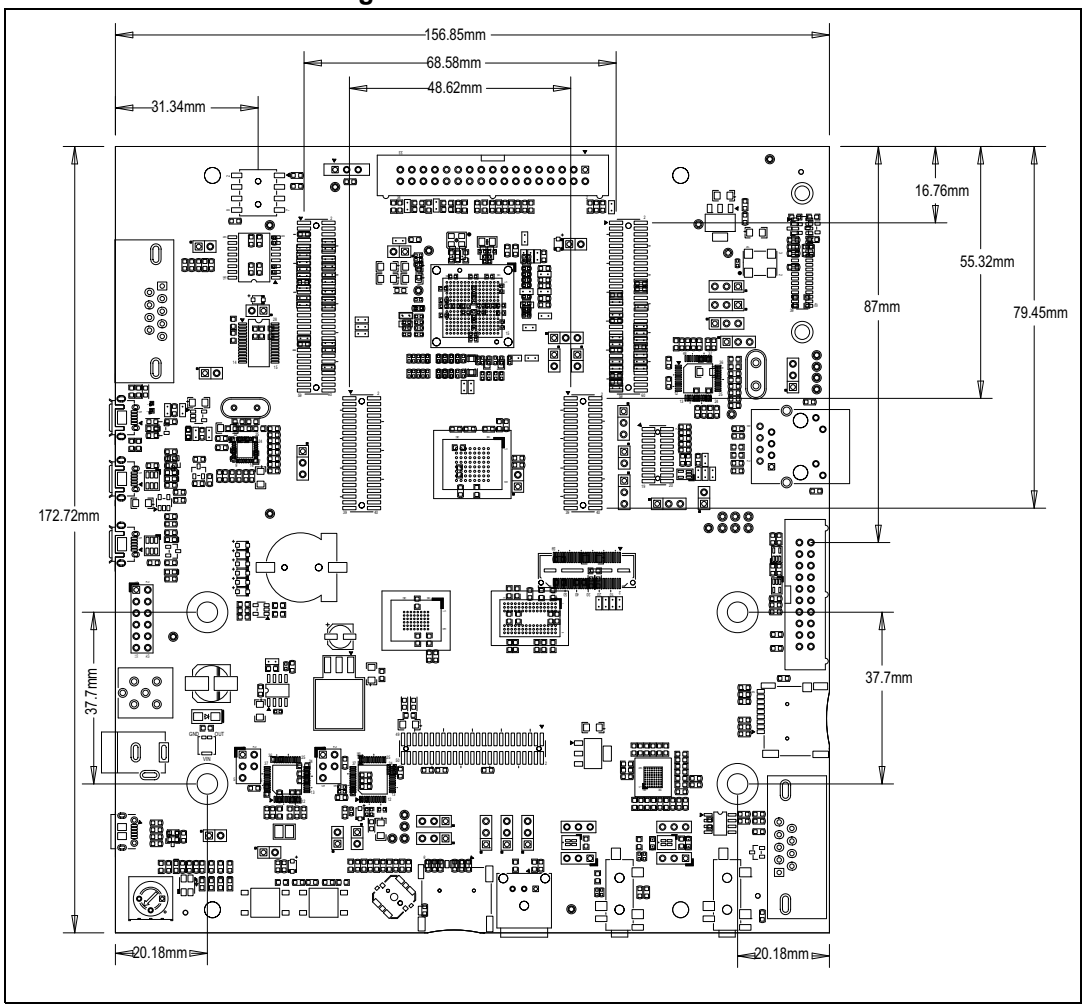


Figure 4. Mechanical dimensions



6.1 Embedded ST-LINK/V2-1

The ST-LINK/V2-1 programming and debugging tool is integrated on the STM32F769I-EVAL evaluation board. Compared to ST-LINK/V2 the changes are listed below.

The new features supported on the ST-LINK/V2-1 are:

- USB software re-enumeration
- Virtual COM port interface on USB
- Mass storage interface on USB
- USB power management request for more than 100 mA power on USB

This feature is no more supported on the ST-LINK/V2-1:

- SWIM interface
- Minimum supported application voltage limited to 3 V

Known limitation:

- Activating the readout protection on ST-LINK/V2-1 target, prevents the target application from running afterwards. The target readout protection must be kept disabled.

For all general information concerning debugging and programming features common between ST-LINK/V2 and ST-LINK/V2-1 versions, refer to *ST-LINK/V2 in-circuit debugger/programmer for STM8 and STM32* User manual (UM1075).

Note: 1 ETM can only work at 50 MHz clock by default because the ETM signals are shared with other peripherals. If a best performance of ETM is required (e.g. 84 MHz/98 MHz), R31, R34, R35, R37, R39, R42, SB7, SB8, SB25, SB27 and SB28, must be removed to reduce the stub on the ETM signals. In this way SAI, Ethernet and camera are not functional and NOR Flash and SRAM addresses are limited to A18.

Note: 2 When JP28 is open, the NRST of the ST-LINK MCU (U21) is pulled high. When JP28 is closed, ST-LINK MCU is reset.

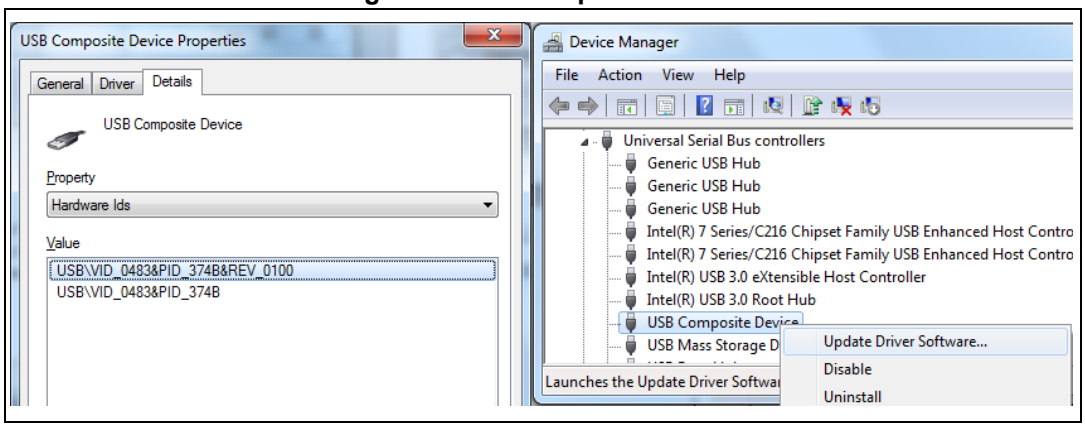
6.1.1 Drivers

Before connecting the STM32F769I-EVAL evaluation board to a Windows 7, Windows 8 or Windows XP PC via USB, a driver for ST-LINK/V2-1 must be installed. It can be downloaded from the *www.st.com* website.

In case the STM32F769I-EVAL evaluation board is connected to the PC before installing the driver, the PC device manager may report some STM32F769I-EVAL interfaces as “Unknown”. To recover from this situation, after installing the dedicated driver, the association of “Unknown” USB devices found on the STM32F769I-EVAL evaluation board to this dedicated driver, must be updated in the device manager manually.

Note: It is recommended to proceed using USB Composite Device, as shown in Figure 5.

Figure 5. USB composite device



6.1.2 ST-LINK/V2-1 firmware upgrade

The ST-LINK/V2-1 embeds a firmware upgrade mechanism for in-situ upgrade through the USB port. As the firmware may evolve during the life time of the ST-LINK/V2-1 product (for example a new functionality, bug fixes, support for new microcontroller families), it is recommended to visit the *www.st.com* website before starting to use the STM32F769I-EVAL board and periodically, to stay up-to-date with the latest firmware version.

6.2 Power supply

The STM32F769I-EVAL evaluation board is designed to be powered by the 5 V DC power supply and to be protected from wrong power plug-in event by PolyZen. It is possible to configure the evaluation board to use any of the following power supply six sources:

- 5 V DC power adapter connected to CN19 (JP20 jumper in position PSU). This is default setting of power supply source selection on STM32F769I-EVAL evaluation board.
- 5 V DC power with 500mA limitation from CN22 (JP20 jumper in position STLK) (the USB Micro-B connector of the ST-LINK/V2-1 that is showed as STLK on JP20 silkscreen and called U5V). If the USB enumeration succeeds (as explained below), the ST-LINK U5V power is enabled, by asserting the PWR_EN pin. This pin is connected to a power switch (ST890), which powers the board. This power switch features also a current limitation to protect the PC in case of short-circuit. If overcurrent (more than 600 mA) happens on the board, the LED LD11 is lit.
- 5 V DC power with 500 mA limitation from CN8 (the USB OTG2 HS Micro-AB connector (JP20 jumper in position HS).
- 5 V DC power with 500 mA limitation from CN13, the USB OTG1 FS Micro-AB connector (JP20 jumper in position FS1).
- 5 V DC power with 500 mA limitation from CN14, the USB OTG2 FS Micro-AB connector (JP20 jumper in position FS2).
- 5 V DC power from CN5 and CN6 (JP20 jumper in position D5V).

The STM32F769I-EVAL evaluation board can be powered from ST-LINK USB Micro-B connector CN22 (U5V), but only the ST-LINK circuit has the power before USB enumeration starting, because the host PC only provides 100 mA to the boards at that time. During the USB enumeration, the STM32F769I-EVAL board asks for the 300 mA power from the host PC. If the host is able to provide the required power, the target STM32 is powered and the red LED LD10 is turned on, thus the STM32F769I-EVAL board can consume maximum 300 mA current, but not more. If the host is not able to provide the requested current, the enumeration fails. Therefore the STM32 part including the extension board will not be powered. As a consequence the red LED LD10 remains turned off. In this case it is mandatory to use an external power supply as an extra power supply.

E5V (from PSU) or D5V must be used as external power supply in case current consumption of STM32F769I-EVAL board exceeds the allowed current on USB. In this condition it is still possible to use USB for communication, for programming or debugging only, but it is mandatory to power the board first using E5V or D5V, and then connecting the USB cable to the PC. Proceeding this way, ensures that the enumeration succeeds thanks to the external power source.

The following power sequence procedure must be respected:

1. Connect jumper JP20 for PSU or D5V side
2. Check that JP27 is removed
3. Connect the external power source to PSU or D5V (daughterboard mounted)
4. Check that the red LED LD10 is turned ON
5. Connect the PC to USB Micro-B connector CN22

If this order is not respected, the board may be powered by VBUS first, then by E5V or D5V, and the following risks may be encountered:

1. If more than 300 mA current is needed by the board, the PC may be damaged or the current can be limited by PC. As a consequence the board is not supplied correctly.
2. 300 mA will be requested at enumeration (since JP27 must be off), so there is the risk that the request is rejected and the enumeration does not succeed if the PC cannot provide such current. Consequently the board is not powered (LED LD10 remains off).

Note: In case the board is powered by a USB charger, there is no USB enumeration, so the led LD10 remains set to off permanently and the board is not powered. In this specific case only the jumper JP27 must be set to on, to allow the board to be powered anyway but in any case the current will be limited to 600 mA by U17 (ST890).

The power supply is configured by setting the related jumpers **JP2, JP15 and JP20** as described in *Table 2*.

Table 2. Power-supply-related jumper settings

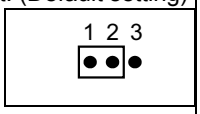
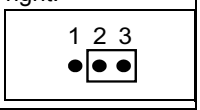
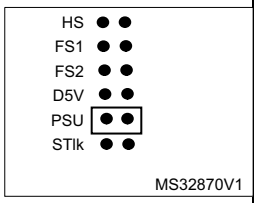
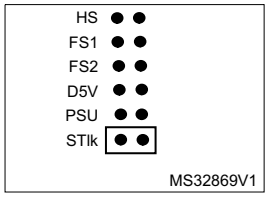
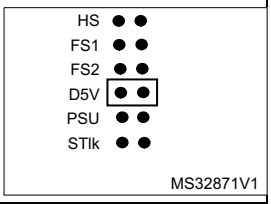
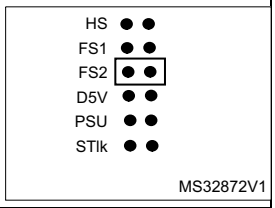
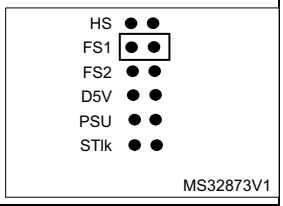
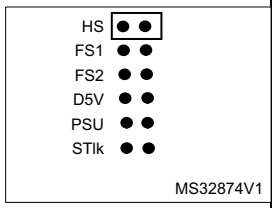
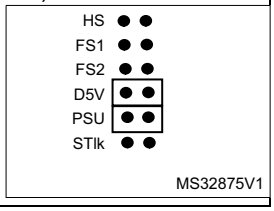
Jumper	Description
JP2	JP2 is used to measure the STM32 current consumption manually by multimeter. Default setting: Fitted
JP15	V_{bat} is connected to +3.3 V when JP15 is set, as shown to the right: (Default setting) 
	V_{bat} is connected to the battery when JP15 is set, as shown to the right: 
JP20	JP20 is used to select one of the six possible power supply resources. STM32F769I-EVAL is supplied through the jack CN19, when JP20 is set as shown to the right: (Default Setting) 
	STM32F769I-EVAL is supplied through the USB connector of the ST-LINK MCU, when JP20 is set as shown on the right: (Default Setting) 

Table 2. Power-supply-related jumper settings (continued)

Jumper	Description
JP20	STM32F769I-EVAL is supplied from the daughterboard connectors (CN5 and CN6) when JP20 is set as shown on the right: 
	STM32F769I-EVAL is supplied from the USB OTG2 FS (CN14),when JP20 is set as shown on the right: 
	STM32F769I-EVAL is supplied from the USB OTG1 FS (CN13), when JP20 is set as shown on the right: 
	STM32F769I-EVAL is supplied from the USB OTG2 HS (CN8) when JP20 is set as shown to the right: 
	STM32F769I-EVAL is supplied from power supply jack (CN19) and daughterboard connected on CN5 and CN6, when JP20 is set as shown on the right (daughterboard must not have its own power supply connected). 

The LED LD10 is lit when the STM32F769I-EVAL evaluation board is powered by the 5 V correctly.

To avoid the impact of USB PHY and Ethernet PHY and get precise results of current consumption on JP2, the following cautions must be taken into account:

1. Configure Ethernet PHY into Power Down Mode by setting low level of IO_Expander (EXP_IO1)
2. Configure USB HS PHY into Low-power mode (Register address = 04, bit 6 in USB PHY).

6.3 Clock source

Five clock sources are available on the STM32F769I-EVAL board:

- X1, 25 MHz crystal for the HSE of the STM32F769NI
- X2, 32 KHz crystal for embedded RTC of the STM32F769NI
- X3, 24 MHz oscillator for camera module (Default on camera daughterboard)
- X4, 25 MHz crystal with socket for Ethernet PHY
- X5, 24 MHz crystal for USB OTG2 HS PHY

Table 3. 25 MHz crystal X1 related solder bridges

Jumper	Description
SB40	PH0 is connected to 25 MHz crystal when SB40 is open. (Default setting)
	PH0 is connected to extension connector CN5 when SB40 is closed. In such case C23, X1 must be removed to avoid disturbance due to the 25 MHz quartz.
SB41	PH1 is connected to 25 MHz crystal when SB41 is open. (Default setting)
	PH1 is connected to extension connector CN5 when SB41 is closed. In such case R20 must be removed to avoid disturbance due to the 25 MHz quartz.

Table 4. 32 KHz crystal X2 related solder bridges

Solder bridge	Description
SB38	PC14 is connected to 32 KHz crystal when SB38 is open. (Default setting)
	PC14 is connected to extension connector CN6 when SB38 is closed. In such case R23 must be removed to avoid disturbance due to the 32 Khz quartz.
SB39	PC15 is connected to 32 KHz crystal when SB39 is open. (Default setting)
	PC15 is connected to extension connector CN6 when SB39 is closed. In such case R22 must be removed to avoid disturbance due to the 32 Khz quartz.

Note: Jumper JP12 for Ethernet clock refers to Section 6.12: Ethernet.

6.4 Reset source

The reset signal of the STM32F769I-EVAL evaluation board is active low and the reset sources include:

- Reset button B1
- Debugging tools from JTAG/SWD connector CN16 and ETM trace connector CN12
- Daughterboard from CN5
- Embedded ST-LINK/V2-1
- RS232 connector CN7 pin 8 for ISP.

Note: The jumper JP5 must be closed when the RESET is handled by the CN7 pin 8 of the RS-232 connector (CTS signal).

6.5 Boot option

The STM32F769I-EVAL evaluation board can boot from:

- Embedded user Flash memory
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by setting the switch SW1 (BOOT) and the boot base address programmed in the BOOT_ADD0 and BOOT_ADD1 option bytes. The BOOT can be configured also via RS-232 connector CN7.

Table 5. Boot related switch

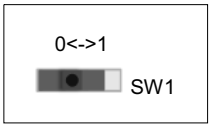
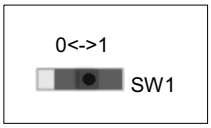
Switch configuration	Boot address option bytes	Boot space
	BOOT_ADD0 [15:0]	STM32F769I-EVAL boot from **BOOT_ADD0[15:0]** **ST programmed value: Flash on ITCM at 0x0020 0000**. (Default setting)
	BOOT_ADD1 [15:0]	STM32F769I-EVAL boot from **BOOT_ADD1[15:0]** ST programmed value: System boot loader at 0x0010 0000

Table 6. Boot related jumpers

Jumper	Description
JP1	The Bootloader_BOOT is managed by pin 6 of connector CN7 (RS232 DSR signal) when JP1 is closed. This configuration is used for boot loader application only. Default Setting: Not fitted

Note: R124 must be removed when boot loader starts up.This prevents the USB_PHY continuous clock from interfering with the USART Rx IOs and the SPI Clock IOs.

6.6 Audio

An audio codec WM8994ECS/R with 4 DACs and 2 ADCs inside is connected to SAI interface of the STM32F769NI to support TDM feature on SAI port. This feature is able to implement audio recording on digital and analog microphone and audio playback of different audio streams on headphone and line-out at the same time.

It communicates with the STM32F769NI via I2C1 bus which is shared with LCD, camera module, and MFX (Multi-Function expander).

The analog microphone on the headset is connected to ADC of WM8994ECS/R through the audio jack CN28. External speakers can be connected to WM8994ECS/R via the audio jack CN27.

Two digital microphones (MEMS microphone) MP34DT01TR are available on the STM32F769I-EVAL evaluation board. They can be connected to either the audio codec or the DFSDM port of the STM32F769NI by setting jumpers shown in *Table 7: Audio related jumpers*. The coupon connectors CN24 and CN25 can be used to support MEMS microphone evaluation board STEVAL-MKI129V1 after removing SB78 and SB79.

An optical connector CN29 is implemented on the STM32F769I-EVAL to receive external audio data which is compatible with SPDIF spec.

Table 7. Audio related jumpers

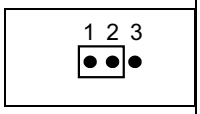
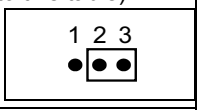
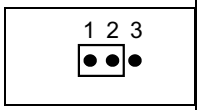
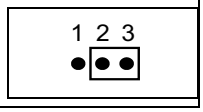
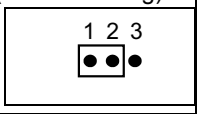
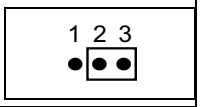
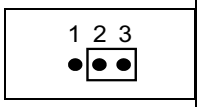
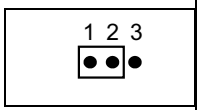
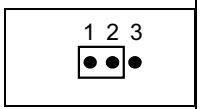
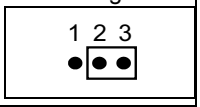
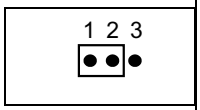
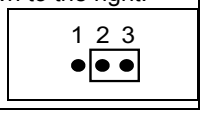
Jumper	Description
JP23	Data signal on digital microphone is connected to audio codec when JP23 is set as shown to the right (Default setting) 
	Data signal on digital microphone is connected to DFSDM of STM32F769NI when JP23 is set as shown to the right (Also need to set JP7 according to this table): 
JP24	Clock signal on digital microphone is connected to audio codec when JP24 is set as shown to the right (Default setting) 
	Clock signal on digital microphone is connected to DFSDM of STM32F769NI when JP24 is set as shown to the right 

Table 7. Audio related jumpers (continued)

Jumper	Description
JP7	PD6 is as SD2_CLK signal when JP7 is set as shown to the right (Default setting): 
	PD6 is connected to DFSDM_DATA1 when JP7 is set as shown to the right (Also need to set JP23 together according to this table): 
JP22	Digital microphone power source is connected to +3.3V power when JP22 is set as shown to the right (Default setting): 
	Digital microphone power source is connected to MICBIAS1 from WM8994ECS/R when JP22 is set as shown to the right: 
JP3	PA2 is connected to SAI2_SCKB when JP3 is set as shown to the right (Default setting): 
	PA2 is connected to MII_MDIO (Ethernet) when JP3 is set as shown to the right: 
JP6	PC1 is connected to SAI1_SDA when JP6 is set as shown to the right (Default setting): 
	PC1 is connected to MII_MDC (Ethernet) when JP6 is set as shown to the right. 

Note: I^2C address of WM8994ECS/R is 0b0011010.

6.7 USB OTG1 FS

The STM32F769I-EVAL evaluation board supports the USB OTG1 full speed communication via a USB Micro-AB connector (CN13) and a USB power switch (U11) connected to VBUS. The evaluation board can be powered through this USB connector with 5 V DC and with 500 mA current limitation.

A green LED LD7 is lit in one of these two cases:

- Power switch (U11) is ON and STM32F769I-EVAL works as a USB host
- VBUS is powered by another USB host when the STM32F769I-EVAL works as a USB device.

The red LED LD8 is lit when overcurrent occurs.

Note: 1 STM32F769I-EVAL board should be powered by an external power supply when using OTG function.

Note: 2 JP14 must be removed when using USB OTG FS, as mentioned in Table 10: CAN related jumpers.

Note: 3 ESDA6V1BC6 (D5) is not entirely securing USB pins against ESD. A negative ESD pulse on the USB pins can result in possible damage to the microcontroller by driving overcurrent through the internal diode of the STM32F769NI.

6.8 USB OTG2 HS and FS

The STM32F769I-EVAL evaluation board supports USB OTG2:

- High speed communication via a USB Micro-AB connector (CN8), USB high-speed PHY (U8) for high-speed function
- Full speed communication via another USB Micro-AB connector (CN14)

The evaluation board can be powered by these USB connectors (CN8 or CN14) at 5 V DC with 500mA current limitation.

As several OTG2 FS signals are shared with OTG2 HS ULPI bus, some PCB reworks are needed, when using OTG2 FS (CN14), as shown in *Table 8*.

Table 8. USB OTG2 function configuration

Function	Mount	Remove
OTG2 HS-CN8 (Default)	R107,R113,SB24,SB21	R263,SB22,SB23,SB65
OTG2 FS-CN14	R263,SB22,SB23,SB65	R107,R113,SB21,SB24

A USB power switch (U7) is also connected on VBUS and provides power to either CN8 (with SB21 and SB24 closed and SB22 and SB23 open) or CN14 (with SB22 and SB23 closed and SB21 and SB24 open).

Green LED LD5 (for CN8) or LD9 (for CN14) is lit when either power switch (U7) is ON and the STM32F769I-EVAL works as a USB host or VBUS is powered by another USB host, when the STM32F769I-EVAL works as a USB device.

The red LED LD6 is lit when overcurrent occurs.

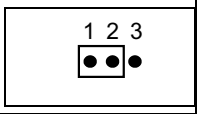
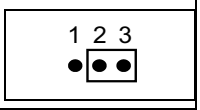
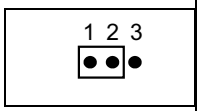
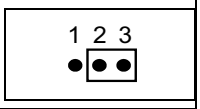
Note: The STM32F769I-EVAL board should be powered by external power supply when using OTG function.

6.9 RS-232

RS-232 communication is supported by D-type 9-pins RS-232 connector CN7, which is connected to the USART1 of the STM32F769NI on the STM32F769I-EVAL evaluation board. The signal Bootloader_RESET and Bootloader_BOOT0 are added on the RS-232 connector CN7 for ISP support.

The USART1 of the STM32F769NI is shared with the RS-232 and the ST-LINK/V2-1 controller. Its communication can be changed by setting JP21 and JP26.

Table 9. USART1 related jumpers

Jumper	Description
JP21	USART1_RX is connected to RS232 when JP21 is set as shown to the right (Default setting, need close JP11 at the same time): 
	USART1_RX is connected to ST-LINK/V2-1 controller's USART_TX when JP21 is set as shown to the right: 
JP26	USART1_TX is connected to RS232 when JP26 is set as shown to the right (Default setting): 
	USART1_TX is connected to ST-LINK/V2-1 controller's USART_RX when JP26 is set as shown to the right: 
JP11	JP11 is used to disconnect MCU and RS232 transceiver chip. Default setting: Fitted

6.10 microSD cards

The two 4-Gbyte (or more) microSD cards connected to SDMMC1 and SDMMC2 ports of the STM32F769NI are available on the board. microSD card1 detection is managed by MFX GPIO15 and microSD card2 detection is managed by MFX GPIO10.

Some PCB reworks are needed for microSD card1 application to disconnect peripherals which share I/Os with microSD card1, and remove the camera module from the board:

- Open SB17, SB72
- Close SB75, SB76

Some PCB reworks are needed for microSD card2 application to disconnect peripherals which share I/Os with microSD card2 and remove the camera module away from the board:

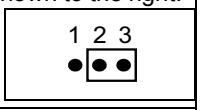
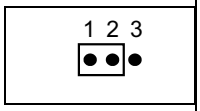
- Open SB16
- Connect JP7 to pin1 and pin 2

6.11 CAN

The STM32F769I-EVAL evaluation board supports one channel of CAN2.0A/B compliant CAN bus communication based on 3.3V CAN transceiver.

High-speed mode, stand-by mode and slope-control mode are available and can be selected by setting JP19.

Table 10. CAN related jumpers

Jumper	Description
JP19	CAN transceiver is working in standby mode when JP19 is set as shown to the right: 
	CAN transceiver is working in high-speed mode when JP19 is set as shown to the right: (default setting) 
	CAN transceiver is working in slope control mode when JP19 is open.
JP18	CAN terminal resistor is enabled when JP18 is fitted. Default setting: Not fitted
JP14	PA11 is connected with CAN RX signal when JP14 is fitted. Default setting: Not fitted

6.12 Ethernet

The STM32F769I-EVAL evaluation board supports 10M/100M Ethernet communication by a PHY DP83848CVV (U6) and integrated RJ45 connector (CN9). Ethernet PHY is connected to STM32F769NI via MII interface.

25M clock can be generated by PHY or provided by MCO from STM32F769NI by setting jumper JP12 shown in *Table 11: Ethernet related jumpers*.

MII serial management signals (MDIO and MDC) are simulated by GPIOs (PJ12 and PJ13) by default on the STM32F769I-EVAL. The original MII serial management signals of the Ethernet IP in the STM32F769NI can be also used by setting JP3 and JP6. Refer *Table 7: Audio related jumpers* for all the details.

Table 11. Ethernet related jumpers

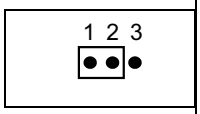
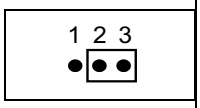
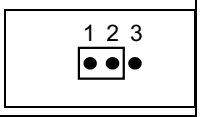
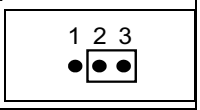
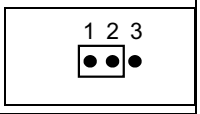
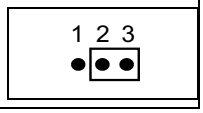
Jumper	Description
JP12	25MHz clock is provided by external crystal X4 when JP12 is set as shown to the right: (Default setting) 
	25MHz clock for MII is provided by MCO at PA8 when JP12 is set as shown to the right: 
JP4	MDIO connect to MII_MDIO_GPIO when JP4 is set as shown to the right: (Default setting) 
	MDIO connect to MII_MDIO when JP4 is set as shown to the right: 
JP8	MDC connect to MII_MDC when JP8 is set as shown to the right: 
	MDC connect to MII_MDC_GPIO when JP8 is set as shown to the right: (Default setting) 

Table 12. Ethernet related solder bridges

Solder bridges	Description
SB47	MII CRS on DP83848CVV is connected to PA0 when SB47 is closed and SB43, SB45 are open. Default setting: Open
SB58	MII COL on DP83848CVV is connected to PH3 when SB58 is closed and R255 is unmounted. Default setting: Open
SB12	MII_RX_ER on DP83848CVV is connected to PI10 when SB12 is closed and R252 is unmounted. Default setting: Open

6.13 Memories

8M x 32bit SDRAM is connected to the SDRAM bank1 of the FMC interface of the STM32F769NI.

1Mx16bit SRAM is connected to the NOR/PSRAM2 bank1 of the FMC interface and both 8-bit and 16-bit accesses are allowed by BLN0 and BLN1 connected to BLE and BHE of the SRAM respectively.

The 128-Mbit NOR Flash memory is connected to the NOR/PSRAM1 bank1 of the FMC interface. The 16-bit operation mode is selected by pull-up resistor connected to BYTE pin of the NOR Flash memory. The write protection can be enabled or disabled depending on how the jumper JP16 is set, as shown in *Table 13*:

Table 13. NOR Flash related jumpers

Jumper	Description
JP16	Write protection is enabled when JP16 is fitted while write protection is disabled when JP16 is not fitted. Default Setting: Not fitted
JP9	PC6 is connected with FMC_NWAIT signal when JP9 is fitted
JP10	PC7 is connected with FMC_NE1 signal when JP10 is fitted

All signals for memory are also connected on memory connectors CN10 and CN11 for memory daughterboards.

Some addressing limitations can happen on FMC when using other peripherals.

FMC addresses are limited to:

- A21 when SAI used
- A20 when camera is used
- A22 when Ethernet is used
- A20 when RGB LCD is used
- A18 for 4-bit ETM to A21 for 1-bit ETM when the ETM trace is used

In such cases, memory addresses A19 to A22 not connected to FMC are pulled down, so that memories can be addressed within a limited address range. If A21 or A22 is required, the camera board should be removed from the STM32F769I-EVAL board.

6.14 Quad-SPI NOR Flash

The 512-Mbit Quad-SPI NOR Flash is connected to Quad-SPI interface of the STM32F769NI on the STM32F769I-EVAL evaluation board.

6.15 Analog input

The two-pin header CN3 and 10K ohm potentiometer RV1 is connected to PF10 of the STM32F769NI as analog input. A low pass filter can be implemented by replacing R29 and C24 with the right value of the resistor and the capacitor, as requested by end user’s application.

6.16 Camera module

A connector CN4 for DCMI signals is on STM32F769I-EVAL evaluation board and camera module daughterboard MB1183.

DCMI signals are duplicated with other peripherals (SAI, I^2S, NOR Flash, microSD cards, trace and MEMS microphone). These peripherals may not function correctly if camera module is being used.

PC7 is shared between PAR_D1 of the camera and the EN pin of the NOR flash. As a consequence when the camera is working, JP10 must be opened to avoid conflicts between NOR Flash and camera.

6.17 Display and input devices

The 4-inch 800x480 TFT color LCD with capacitive touch panel is connected to MIPI DSI interface of the STM32F769NI. Users can connect MB1232 to DSI LCD connector CN15, to convert the DSI interface to the HDMI interface; users can also connect MB1233 to CN15 to use RaspberryPI LCD.

Four general purpose color LEDs (LD1, 2, 3 and 4) are available as display devices and they are connected respectively to PI15, PJ0, PJ1, and PJ3 of the STM32F769NI.

The 4-direction joystick (B3) is connected to the MFX.

User button (B2) is connected to PC13 which supports Wakeup or Tamper feature.

Table 14. DSI LCD modules connector (CN15)

Pin No.	Description	Pin connection	Pin No.	Description	Pin connection
1	GND	-	2	-	-
3	DSI_CK_P	-	4	TOUCH_INT	MFX GPIO14
5	DSI_CK_N	-	6	GND	-
7	GND	-	8	DSI_D2_P/GND	-
9	DSI_D0_P	-	10	DSI_D2_N/GND	-
11	DSI_D0_N	-	12	GND	-
13	GND	-	14	DSI_D3_P/GND	-
15	DSI_D1_P	-	16	DSI_D3_N/GND	-
17	DSI_D1_N	-	18	GND	-
19	GND	-	20	-	-
21	BLVDD(5 V)	-	22	-	-
23	BLVDD(5 V)	-	24	-	-
25	-	-	26	-	-
27	BLGND	-	28	-	-
29	BLGND	-	30	-	-
31	-	-	32	-	-
33	-	-	34	-	-

Table 14. DSI LCD modules connector (CN15) (continued)

Pin No.	Description	Pin connection	Pin No.	Description	Pin connection
35	SCLK/MCLK	-	36	3.3V	-
37	LRCLK	-	38	-	-
39	SPDIF/I^{2}S	-	40	I2C1_SDA	PB9
41	-	-	42	-	-
43	-	-	44	I2C1_SCL	PB8
45	CEC_CLK	-	46	-	-
47	CEC	-	48	-	-
49	DSI_TE	PJ2	50	-	-
51	-	-	52	-	-
53	BL_CTRL	PA8	54	-	-
55	-	-	56	-	-
57	DSI_RESET	PK7	58	-	-
59	-	-	60	1V8	-

6.18 Motor control

The STM32F769I-EVAL evaluation board supports both asynchronous and synchronous three-phase brushless motor control via a 34-pin connector CN1, which provides all required control and feedback signals to and from the motor-power-driving board.

Available signals on this connector include emergency stop, motor speed, 3-phase motor current, bus voltage, heatsink temperature coming from the motor driving board and six channels of PWM control signal going to the motor driving circuit.

To enable motors control applications, some reworks are needed to disconnect the peripherals, which share I/Os with the motor control connector, and to connect these I/Os to the motor control connector:

- Solder bridges to be opened:
  - SB3, SB36, SB43, SB47, SB48, SB52, SB54, SB55, SB62, SB66, SB69, SB71, SB74, SB17, SB75, remove R93, R98, R245, R256
- Keep no jumper on JP3/JP6/JP9/JP10/JP14
- Keep CN4 and CN13 unconnected
- Solder bridges to be closed:
  - SB34, SB37, SB42, SB45, SB46, SB49, SB50, SB51, SB53, SB56, SB57, SB60, SB64, SB67, SB70, SB72, SB73, SB18
- Mount R14 with 0 ohm resistor.

PA4 and PA5 are DAC outputs when using them for debugging purposes, keep CN4 unconnected and remove R124.

In *Figure 6* and *Figure 7* the components which need to be removed are marked in red, while the ones that need to be in place are marked in green.

Figure 6. STM32F769I-EVAL evaluation board motor control PCB reworks (Top side)

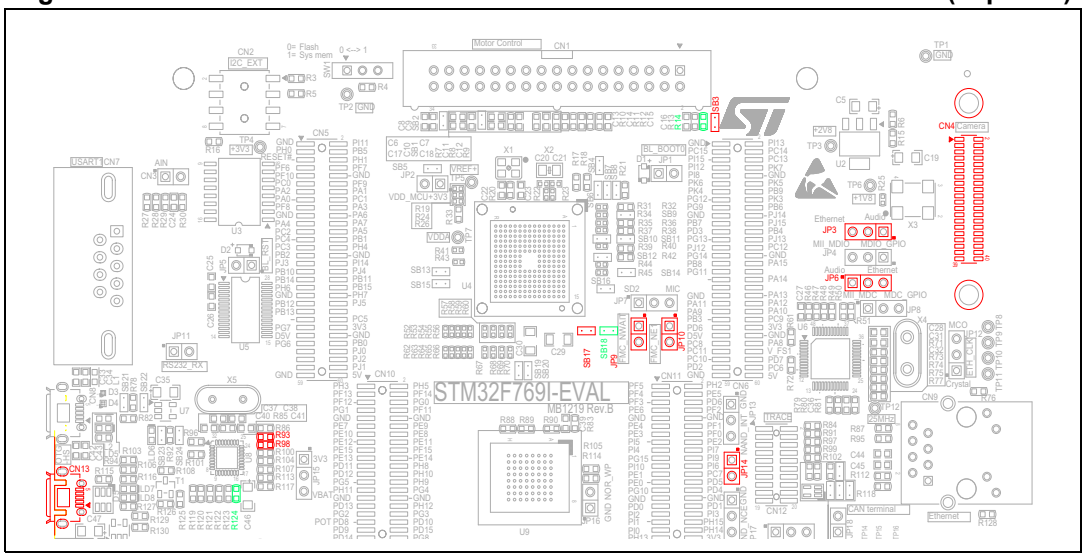


Figure 7. STM32F769I-EVAL evaluation board motor control PCB reworks (Bottom side)

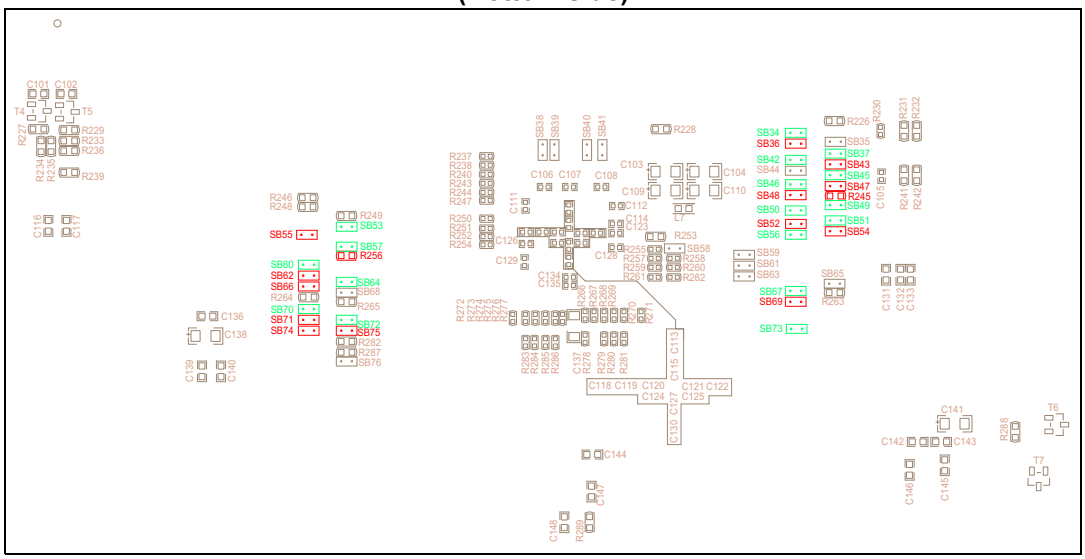


Table 15. Motor control related solder bridges

Solder bridges	Description
SB1	The special motor current sampling operation is enabled when SB1 is closed (PA12 connected to PA8). The I/O pins PA12 and PA8 are disconnected and can be used by the daughterboard when SB1 is not fitted. Default setting: Open
SB2	SB2 should be kept open when encoder signal comes from the pin 31 of the motor control connector CN1, while it should be kept close when analog signal comes from pin 31 of CN1 for special motor. Default setting: Open

6.19 Multi-Function expander

The Multi-Function expander (MFX) is implemented as an I/O expander circuit on the STM32F769I-EVAL evaluation board. The communication interface between MFX and STM32F769NI is done through the I2C1 interface.

The signals connected to MFX are listed in *Table 16: MFX signals* .

Table 16. MFX signals

Pin number of MFX	Pin name of MFX	MFX functions	Function of STM32F769I-EVAL	Direction (For MFX)	Terminal device
10	PA0	MFX_GPO1	XSDN	Output	Camera
15	PA5	MFX_GPIO5	Audio_INT	Input	Codec
16	PA6	MFX_GPIO6	OTG_FS1_ OverCurrent	Input	USB_FS1
17	PA7	MFX_GPIO7	OTG_FS1_ PowerSwitchOn	Output	USB_FS1
18	PB0	MFX_GPIO0	JOY_SEL	Input	Joystick
19	PB1	MFX_GPIO1	JOY_DOWN	Input	Joystick
20	PB2	MFX_GPIO2	JOY_LEFT	Input	Joystick
26	PB13	MFX_GPIO13	MII_INT	Input	Ethernet PHY
27	PB14	MFX_GPIO14	LCD_INT	Input	LCD
28	PB15	MFX_GPIO15	MicroSDcard Detect1	Input	MicroSD1
29	PA8	MFX_GPIO8	OTG_FS2_ OverCurrent	Input	USB_FS2
30	PA9	MFX_GPIO9	OTG_FS2_ PowerSwitchOn	Output	USB_FS2
31	PA10	MFX_GPIO10	MicroSDcard Detect2	Input	MicroSD2
32	PA11	MFX_GPIO11	RSTI	Output	Camera
33	PA12	MFX_GPIO12	Camera_PLUG	Input	Camera
39	PB3	MFX_GPIO3	JOY_RIGHT	Input	Joystick
40	PB4	MFX_GPIO4	JOY_UP	Input	Joystick

7 Connectors

7.1 Motor control connector CN1

Figure 8. Motor control connector CN1 (Top view)

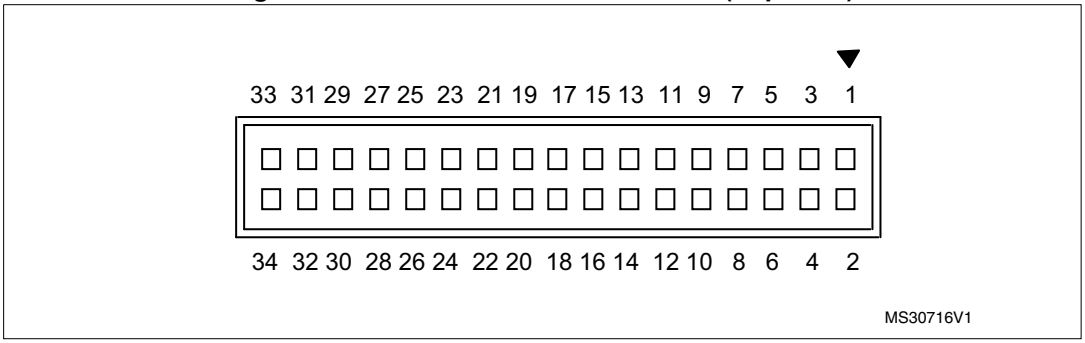


Table 17. Motor control connector CN1

Description	Pin of STM32F769NI	Pin number of CN1	Pin number of CN1	Pin of STM32F769NI	Description
Emergency STOP	PA6	1	2	-	GND
MC_UH	PC6	3	4	-	GND
MC_UL	PA7	5	6	-	GND
MC_VH	PC7	7	8	-	GND
MC_VL	PB0	9	10	-	GND
MC_WH	PC8	11	12	-	GND
MC_WL	PB1	13	14	PC4	BUS VOLTAGE
CURRENT A	PC1	15	16	-	GND
CURRENT B	PC2	17	18	-	GND
CURRENT C	PC3	19	20	-	GND
NTC BYPASS RELAY	PG11	21	22	-	GND
DISSIPATIVE BRAKE PWM	PH6	23	24	-	GND
+5 V power	-	25	26	PC5	Heatsink temperature
PFC SYNC	PA12 and PA8 See *Table 15* for details.	27	28	-	3.3V power
PFC PWM	PA11	29	30	-	GND
Encoder A	PA0	31	32	-	GND
Encoder B	PA1	33	34	PA2	Encoder Index

7.2 I²C connector CN2

Figure 9. I²C connector CN2 (Front view)

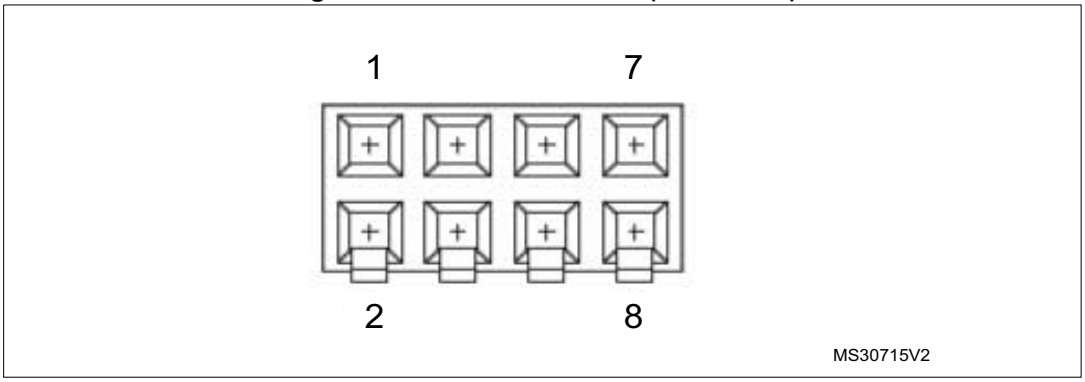


Table 18. I²C connector CN2

Pin number	Description	Pin number	Description
1	I2C1_SDA (PB9)	5	+3V3
2	NC	6	NC
3	I2C1_SCL (PB8)	7	GND
4	RESET (PC10)	8	NC

7.3 Analog input-output connector CN3

Figure 10. Analog input-output connector CN3 (Top view)

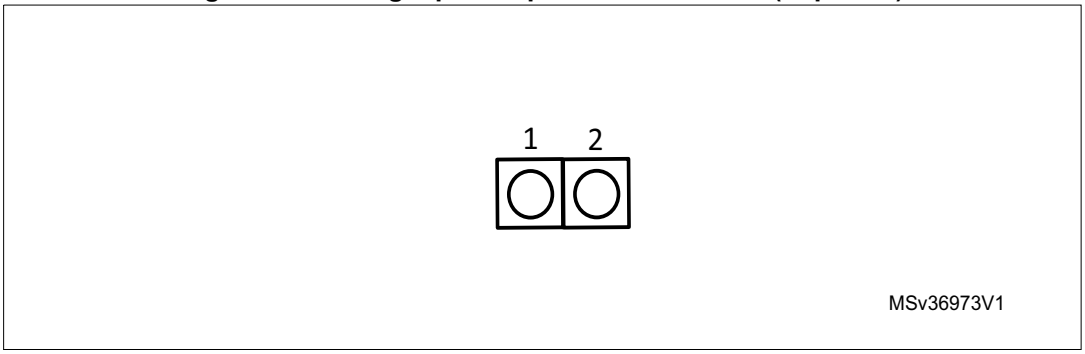


Table 19. Analog input-output connector CN3

Pin number	Description	Pin number	Description
1	analog input-output (PF10)	2	GND

7.4 Camera module connector CN4

Figure 11. Camera module connector CN4 (Top view)

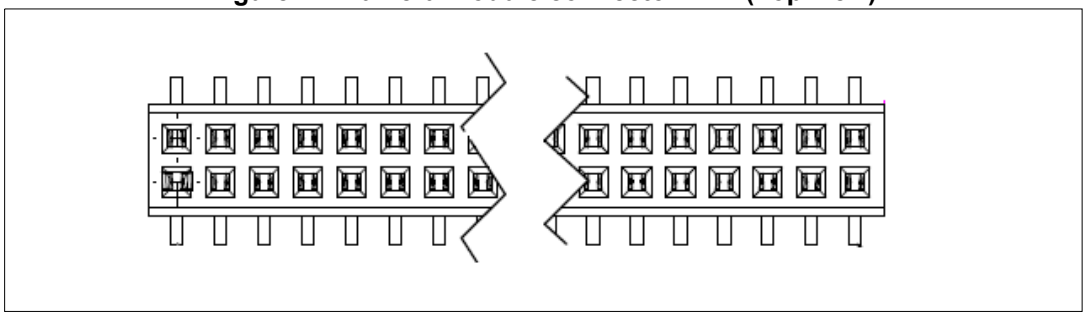


Table 20. Camera module connector CN4

Pin number	Description	Pin number	Description
1	+1.8V	21	GND
2	+1.8V	22	GND
3	GND	23	D0 (PC6)
4	GND	24	D1 (PC7)
5	D10 (PD6)	25	D2 (PC8)
6	D11 (PD2)	26	D3 (PC9)
7	GND	27	D4 (PC11)
8	GND	28	D5 (PD3)
9	D8 (PC10)	29	D6 (PE5)
10	D9 (PC12)	30	D7 (PE6)
11	GND	31	HSYNC (PA4)
12	GND	32	VSYNC (PB7)
13	I2C1_SCL (PB8)	33	PCLK (PA6)
14	I2C1_SDA (PB9)	34	Test point8
15	Camera_PLUG (MFX GPIO12)	35	Test point11
16	GND	36	Test point10
17	RST IN (MFX GPIO11)	37	GND
18	Test point 7	38	GND
19	XSDN (MFX GPIO0)	39	+2.8V
20	Camera clock	40	+2.8V

7.5 Daughterboard extension connectors CN5 and CN6

Two 60-pin male headers CN5 and CN6 can be used to connect a daughterboard or the standard wrapping board to the STM32F769I-EVAL evaluation board. All GPIOs are dispatched on memory connectors (CN10 and CN11), and on connectors CN5 and CN6.

The space between these two connectors is defined as a standard which allows developing common daughterboards for several ST evaluation boards. The standard width between CN5 pin 1 and CN6 pin 1 is 2700mils (68.58mm).

Each pin on CN5 and CN6 can be used by a daughterboard after disconnecting it from the corresponding function block on the STM32F769I-EVAL evaluation board. For more details refer to *Table 21* and *Table 22*.

Table 21. Daughterboard extension connector CN5

Pin	Description	Alternative function	How to disconnect with function block on STM32F769I-EVAL board
1	GND	-	-
3	PH0	OSC_IN	Remove X1,C23, Close SB40
5	RESET#	-	-
7	PF6	QSPI_BK1_IO3	Remove R241
9	PF10	Potentiometer	Remove R30
11	PC0	ULPI_STP	Remove R123
13	PA2	SAI2_SCKB/MII_MDIO/MC_EnIndex	Open SB37, SB35
15	PA0	SAI2_SDB/ MII_CRS/MC_ENA	Open SB43, SB45, SB47
17	PF8	QSPI_BK1_IO0	Remove R242
19	GND	-	-
21	PA4	PAR_HSYNC	Disconnect CN4
23	PC2	MII_TXD2/MC_CurrentB	Open SB49, remove R245
25	PC4	MII_RXD0/ MC_BUSVOLTAGE	Open SB51, SB54
27	PC3	MII_TX_CLK/ MC_CurrentC	Open SB52, SB56
29	PB2	QSPI_CLK	-
31	PJ3	LCD_R4/LED3	Open SB59
33	PB10	ULPI_D3/LCD_G4	Remove R100, open SB63
35	PB14	USB_FS2_DM	Disconnect CN14
37	PH6	MII_RXD2/MC_DissipativeBrake	Open SB53, SB55
39	GND	-	-
41	PB12	ULPI_D5/ USB_FS2_ID	Open SB65, remove R107
43	PB13	ULPI_D6/ USB_FS2_VBUS	Remove R263, R113
45	PJ9	-	-
47	PG7	NAND_INT	Open SB19

Table 21. Daughterboard extension connector CN5 (continued)

Pin	Description	Alternative function	How to disconnect with function block on STM32F769I-EVAL board
49	D5V	-	-
51	PG6	LCD_R7/FMC_NE3	Open SB20
53	PJ7	-	-
55	PJ10	-	-
57	PJ8	-	-
59	GND	-	-
2	PI11	ULPI_DIR	Remove R122
4	PB5	ULPI_D7/LCD_G7	Remove R117, open SB5
6	PH1	OSC_OUT	Remove R20, close SB41
8	PF7	QSPI_BK1_IO2	Remove R232
10	GND	-	-
12	PF9	QSPI_BK1_IO1	Remove R231
14	PA1	MII_RX_CLK/MC_ENB	Open SB34, SB36
16	PC1	SAI1_SDA/MII_MDC/ MC_CurrentA	Open SB42, keep JP6 on open
18	PA3	ULPI_D0	Remove R86
20	PA6	MC_EmergencySTOP/ PAR_PCLK/LCD_G2	Remove SB3, R14
22	PA7	MII_RX_DV/MC_UL	Open SB46, SB48
24	PA5	ULPI_CK	Remove R124
26	PB1	ULPI_D2/MC_WL	Open SB50, remove R98
28	PH4	ULPI_NXT	Remove R121
30	GND	-	-
32	PI14	LCD_CLK	-
34	PJ4	LCD_R5	-
36	PB11	ULPI_D4/LCD_G5	Remove R104, open SB61
38	PB15	USB_FS2_DP	Disconnect CN14
40	PH7	MII_RXD3	Remove R46
42	PJ5	LCD_R6	-
44	PJ6	-	-
46	PC5	MII_RXD1/MC_HEATSINK	Open SB67, SB69
48	+3V3	-	-
50	GND	-	-
52	PB0	ULPI_D1/MC_VL	Open SB73, remove R93
54	PJ0	LCD_R1/LED1	Open SB13

Table 21. Daughterboard extension connector CN5 (continued)

Pin	Description	Alternative function	How to disconnect with function block on STM32F769I-EVAL board
56	PJ2	LCD_R3/DSI_TE	Disconnect CN15
58	PJ1	LCD_R2/LED2	Open SB15
60	+5 V	-	-

Table 22. Daughterboard extension connector CN6

Pin	Description	Alternative Function	How to disconnect with function block on STM32F769I-EVAL board
1	GND	-	-
3	PC15	OSC32_OUT	Remove R22, close SB39
5	PI15	LCD_R0/LED0	Open SB0
7	PI12	LCD_HSYNC	-
9	PI8	EXPANDER_INT	Remove R296
11	PK6	LCD_B7	-
13	PK4	LCD_B5	-
15	PG12	SPDIF_RX1	Remove R206
17	PG9	SAI2_FSB,SD2_D0, LRCLK	Remove R172, disconnect DSI and SD2
19	GND	-	-
21	PB7	LED3/PAR_ VSYNC	Disconnect CN4
23	PD3	DFSDM_CLK	JP24 open
25	PG13	MII_TXD0	Remove R248
27	PJ12	LCD_B0	-
29	PG14	MII_TXD1	Remove R249
31	PB8	I2C1_SCL	Remove R175, R5, R293, disconnect CN4,CN15 and CN18
33	PG11	MII_TX_EN/MC_NTC	Open SB46, remove R252
35	PJ11	-	-
37	PK0	-	-
39	GND	-	-
41	PA11	CAN1_RX/USB_FS1_DM /MC_PFCpwm	Open SB64, keep JP14 on open, disconnect CN13
43	PA9	RS232_TX/USB_FS1_VBUS	Open SB68, remove R265
45	PB3	JTDO- SWO/SD2_D2	Remove R97, disconnect SD2
47	PD6	DFSDM_DATA1/SD2_CLK/PAR_D10	Keep JP7 on open, disconnect CN4 and SD2
49	D5V	-	-

Table 22. Daughterboard extension connector CN6 (continued)

Pin	Description	Alternative Function	How to disconnect with function block on STM32F769I-EVAL board
51	PC8	SD1_D0/MC_WH/PAR_D2	Open SB17 SB72,SB75, disconnect CN4 and SD1
53	PC11	SD1_D3 /PAR_D4	Remove R282, disconnect CN4, disconnect SD1
55	PC10	SD1_D2/EXT_RESET/PAR_D8	Remove R287,R16, disconnect CN4 and SD1
57	PD2	SD1_CMD/PAR_D11	Open SB76, disconnect CN4 and SD1
59	GND	-	-
2	PI13	LCD_VSYNC	-
4	PC14	OSC32_IN	Remove R23, close SB38
6	PC13	TAMPER_WAKEUP_KEY	Remove R217
8	PK7	LCD_ENB	Remove R162, disconnect CN15
10	GND	-	-
12	PK5	LCD_B6	-
14	PB9	I2C1_SDA	Remove R174, R3,R294, disconnect CN4, CN15 and CN18
16	PK3	LCD_B4	-
18	PB6	QSPI_BK1_NCS	Remove R230
20	PJ14	LCD_B2	-
22	PJ15	LCD_B3	-
24	PB4	JTRST/SD2_D3	Open SB16, disconnect SD2
26	PJ13	LCD_B1	-
28	PC12	SD1_CK/ PAR_D9	Disconnect CN4, disconnect SD1
30	GND	-	-
32	PA15	JTDI	Remove R99
34	PK1	-	-
36	PA14	JTCK-SWCLK	Remove R91
38	PK2	-	-
40	PA13	JTMS-SWDIO	Remove R84
42	PA12	CAN1_TX/USB_FS1_DP/MC_PFCsync2	Open SB60, SB62, SB66
44	PA10	RS232_RX/USB_FS1_ID	Remove R115, keep JP21 on open
46	PC9	SD1_D1/PAR_D3	Remove R264, disconnect CN4 and SD1
48	+3.3V	-	-
50	GND	-	-
52	PA8	LCD_BL_CTRL/MII_MCO/MC_PFCsync1	Open SB70, SB71, SB74
54	VBUS_FS1	-	-

Table 22. Daughterboard extension connector CN6 (continued)

Pin	Description	Alternative Function	How to disconnect with function block on STM32F769I-EVAL board
56	PD7	SD2_CMD	Disconnect SD2
58	PC6	MC_UH/PAR_D0/I2S3_CK	Open SB18, disconnect CN4, keep JP9 on open
60	+5 V	-	-

7.6 RS-232 connector CN7

Figure 12. RS-232 connector CN7 (Front view)

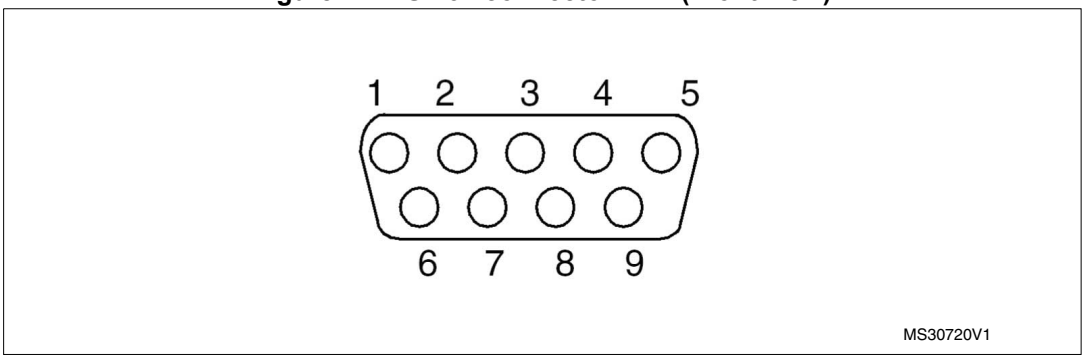


Table 23. RS-232 connector CN7

Pin number	Description	Pin number	Description
1	NC	6	Bootloader_BOOT
2	RS232_RX (PA10)	7	NC
3	RS232_TX (PA9)	8	Bootloader_RESET
4	NC	9	NC
5	GND	-	-

7.7 USB OTG2 HS Micro-AB connector CN8

Figure 13. USB OTG HS Micro-AB connector CN8 (Front view)

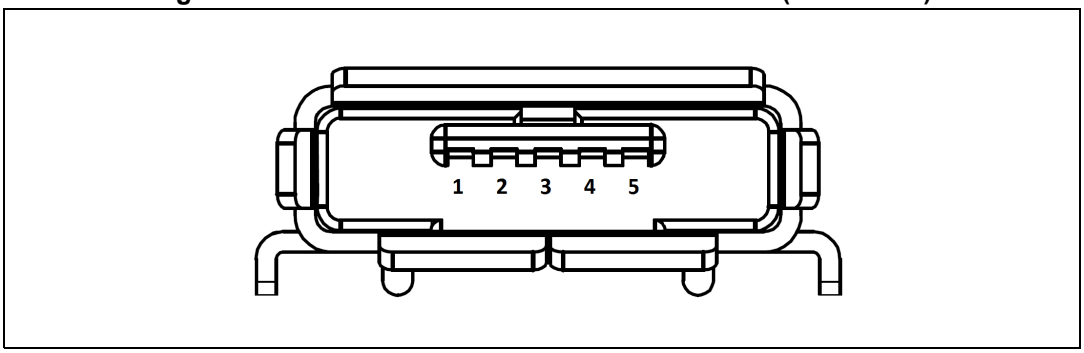


Table 24. USB OTG HS Micro-AB connector CN8

Pin number	Description	Pin number	Description
1	VBUS	4	ID
2	D-	5	GND
3	D+	-	-

7.8 Ethernet RJ45 connector CN9

Figure 14. Ethernet RJ45 connector CN9 (Front view)

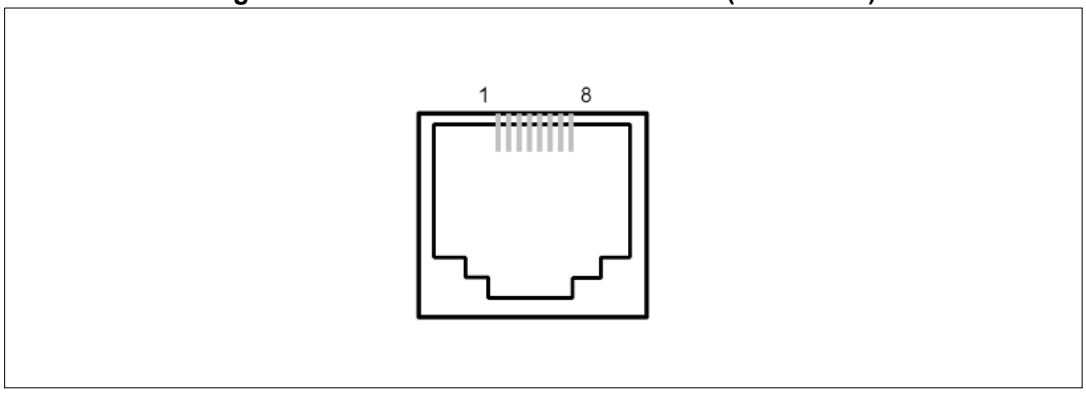


Table 25. RJ45 connector CN9

Pin number	Description	Pin number	Description
1	TxData+	2	TxData-
3	RxData+	4	Shield
5	Shield	6	RxData-
7	Shield	8	Shield

7.9 Memory connector CN10 and CN11

Two 40-pins male headers CN10 and CN11 are used to connect with memory daughterboard. GPIOs (which work as FMC memory signals) that are not present on CN5 and CN6, are available on these two connectors.

The space between these two connectors is defined as a standard which allows to develop common daughterboard. The standard width between CN10 pin 1 and CN11 pin 1 is 1914 mils (48.62 mm). For more details on signal assignment refer to *Table 27* and *Table 28*.

Table 26. Memory connector CN10

Pin	Description	Function	How to disconnect with function block on STM32F769I-EVAL board
1	PH3	SDNE0/MII_COL	Open SB57
3	PF13	A7	-
5	PF12	A6	-
7	PG1	A11	-
9	GND	-	-
11	PE7	D4	-
13	PE10	D7	-
15	PE12	D9	-
17	PE15	D12	-
19	PE13	D10	-
21	PD11	A16	-
23	PD12	A17	-
25	PG5	A15/BA1	-
27	PH11	D19	-
29	GND	-	-
31	PD13	A18	-
33	PG2	A12	-
35	PD8	D13	-
37	PD9	D14	-
39	PD14	D0	-
2	PH5	SDNWE	-
4	PF14	A8	-
6	PG0	A10	-
8	PF11	SDNRAS	-
10	GND	-	-
12	PE9	D6	-
14	PE8	D5	-
16	PE11	D8	-
18	PF15	A9	-
20	PE14	D11	-
22	PH8	D16	-
24	PH10	D18	-
26	PH9	D17	-
28	PG4	A14/BA0	-

Table 26. Memory connector CN10 (continued)

Pin	Description	Function	How to disconnect with function block on STM32F769I-EVAL board
30	GND	-	-
32	PH12	D20	-
34	PG3	A13	-
36	PD10	D15	-
38	PD15	D1	-
40	PG8	SDCLK/ MII_PPS_OUT	-

Table 27. Memory connector CN11

Pin	Description	Alternative function	How to disconnect with function block on STM32F769I-EVAL board
1	PF5	A5	-
3	PF4	A4	-
5	PF3	A3	-
7	PE6	A22/SAI2_MCLK_B/TRACED 3/PAR_D7/LCD_G1	Open SB25, SB26, SB27, SB28
9	GND/PG7	GND/NAND_INT	Short pin 2, 3 of JP13 when connect NAND module to CN11, close SB19, in any other case short pin 1 and 2 of JP13
11	PE4	A20/TRACED1	Open SB11
13	PE3	A19/TRACED0	Open SB9
15	PI5	NBL3	-
17	PI4	NBL2	-
19	PG15	SDNCAS	-
21	PI10	D31/MII_RX_ER	Open SB12
23	PE1	NBL1	-
25	PE0	NBL0	-
27	PG6	NE3/LCD_R7	Close SB20
29	GND	-	-
31	PD0	D2	-
33	PI2	D26	-
35	PI1	D25	-
37	PI0	D24	-
39	PH13	D21	-
2	PH2	SDCKE0	-
4	PE5	A21/TRACED2/PAR_D6/LCD _G0	Open SB6, SB7, SB8

Table 27. Memory connector CN11 (continued)

Pin	Description	Alternative function	How to disconnect with function block on STM32F769I-EVAL board
6	PC6	NWAIT /MC_UH/ PAR_D0	Close JP9, disconnect CN4 and CN1
8	PF2	A2	-
10	GND	-	-
12	PF1	A1	-
14	PF0	A0	-
16	PE2	A23/TRACECLK/ MII_TXD3	Open SB10, remove R42
18	PI7	D29	-
20	PI9	D30	-
22	PI6	D28	-
24	PC7	NE1/MC_VH/ PAR_D0	Connect JP10, disconnect CN4,CN1
26	PD5	NWE	-
28	PD4	NOE	-
30	GND/PC8	GND/NAND_NCE/ PAR_D0	Short pin 2, 3 of JP17, open SB72, SB75, close SB18, disconnect CN4,CN1 when connect NAND module to CN11, in any other case short pin 1, 2 of JP17
32	PD1	D3	-
34	PI3	D27	-
36	PH15	D23	-
38	PH14	D22	-
40	+3.3V	-	-

7.10 ETM trace debugging connector CN12

Figure 15. ETM trace debugging connector CN12 (Top view)

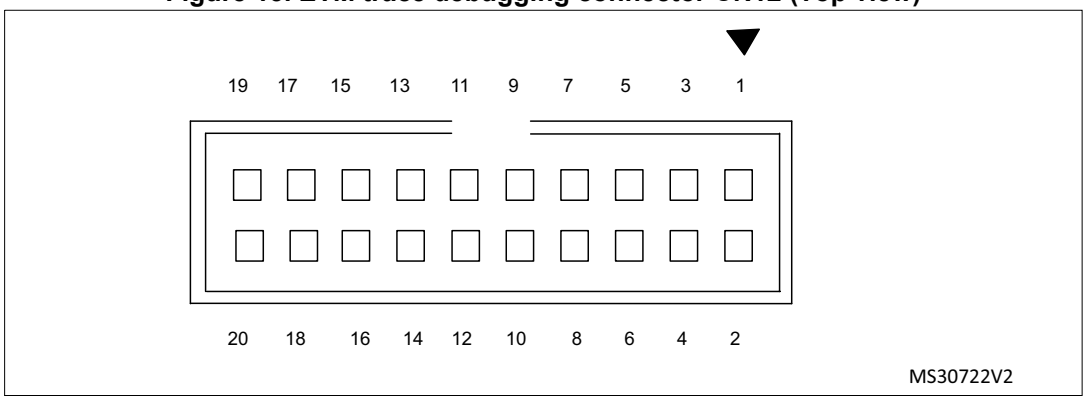


Table 28. ETM trace debugging connector CN12

Pin number	Description	Pin number	Description
1	+3.3V	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	TraceCLK/PE2
13	GND	14	TraceD0/PE3 or SWO/PB3
15	GND	16	TraceD1/PE4 or nTRST/PB4
17	GND	18	TraceD2/PE5
19	GND	20	TraceD3/PE6

7.11 USB OTG1 FS Micro-AB connector CN13

Figure 16. USB OTG1 FS Micro-AB connector CN13 (Front view)

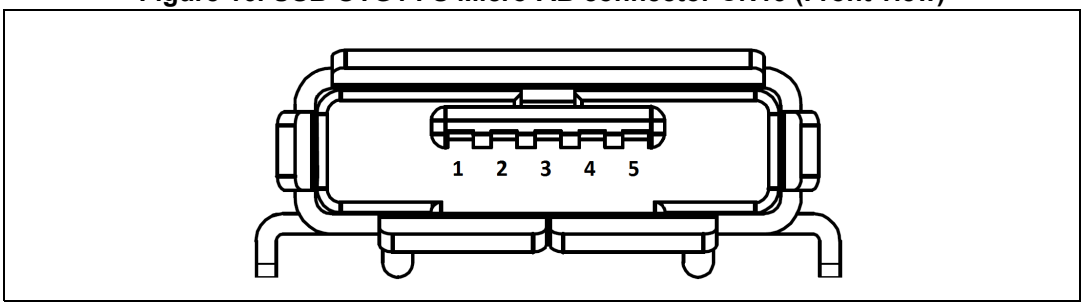


Table 29. USB OTG1 FS Micro-AB connector CN13

Pin number	Description	Pin number	Description
1	VBUS (PA9)	4	ID (PA10)
2	D- (PA11)	5	GND
3	D+ (PA12)	-	-

7.12 USB OTG2 FS Micro-AB connector CN14

Figure 17. USB OTG2 FS Micro-AB connector CN14 (Front view)

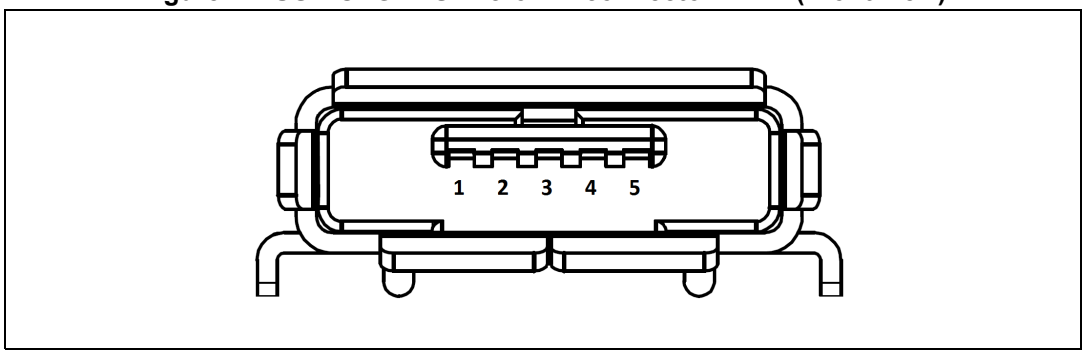


Table 30. USB OTG2 FS Micro-AB connector CN14

Pin number	Description	Pin number	Description
1	VBUS (PB13)	4	ID (PB12)
2	D- (PB14)	5	GND
3	D+ (PB15)	-	-

7.13 JTAG/SWD connector CN16

Figure 18. JTAG/SWD debugging connector CN16 (Top view)

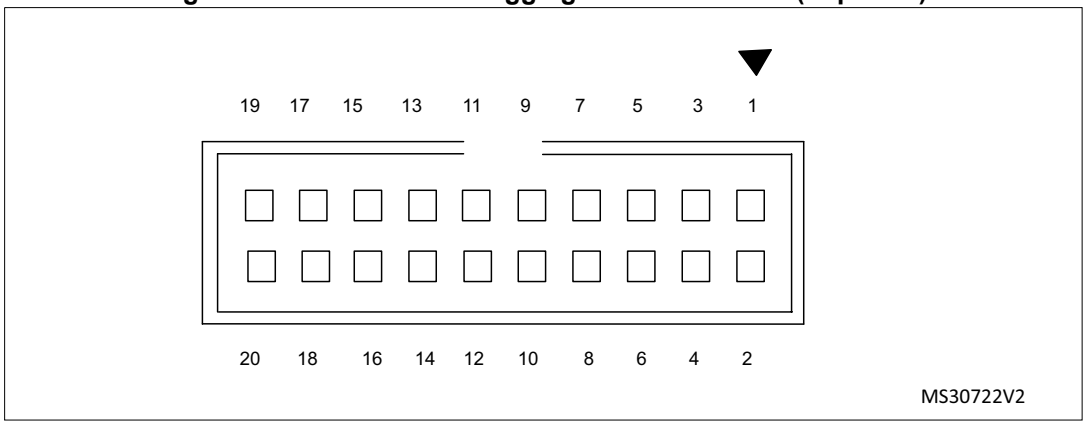


Table 31. JTAG/SWD debugging connector CN16

Pin number	Description	Pin number	Description
1	+3.3V	2	+3.3V
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND

Table 31. JTAG/SWD debugging connector CN16 (continued)

Pin number	Description	Pin number	Description
11	RTCK	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	DBGRQ	18	GND
19	DBGACK	20	GND

7.14 microSD connectors CN17 and CN30

Figure 19. microSD connector (Top view)

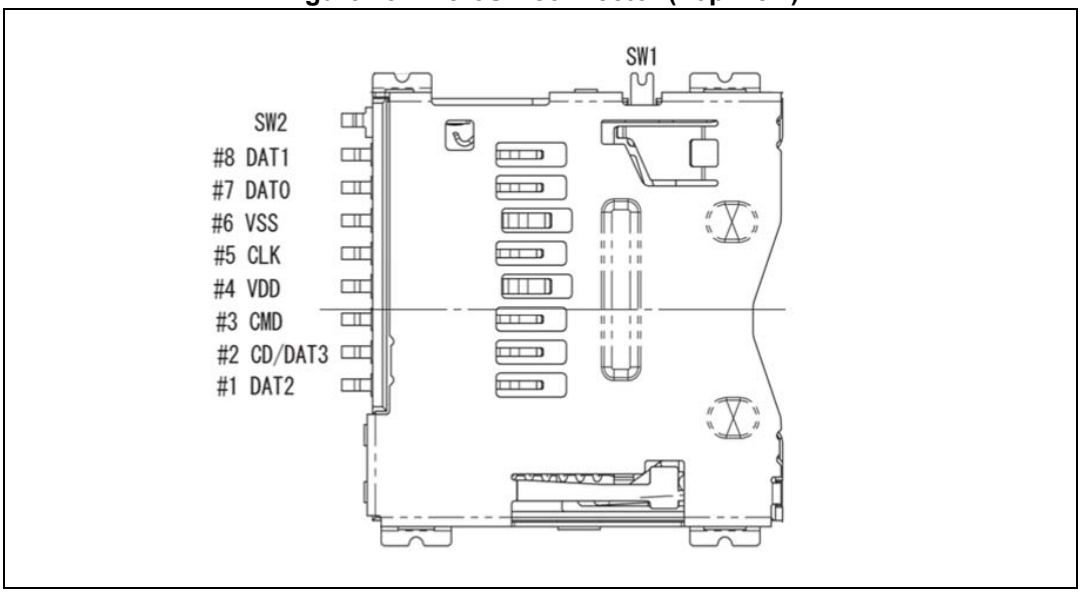


Table 32. microSD card1 connector CN17

Pin number	Description	Pin number	Description
1	SDMMC_D2 (PC10)	6	Vss/GND
2	SDMMC_D3 (PC11)	7	SDMMC_D0 (PC8)
3	SDMMC_CMD (PD2)	8	SDMMC_D1 (PC9)
4	+3.3V	9	GND
5	SDMMC_CLK (PC12)	10	MicroSDcard_detect1 (MFX GPIO15)

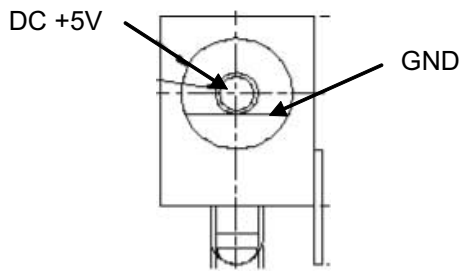
Table 33. microSD card2 connector CN30

Pin number	Description	Pin number	Description
1	SDMMC_D2 (PB3)	6	Vss/GND
2	SDMMC_D3 (PB4)	7	SDMMC_D0 (PG9)
3	SDMMC_CMD (PD7)	8	SDMMC_D1 (PG10)
4	+3.3V	9	GND
5	SDMMC_CLK(PD6)	10	MicroSDcard_detect2 (MFX GPIO10)

7.15 Power connector CN19

STM32F769I-EVAL evaluation board can be powered from a DC 5V power supply via the external power supply jack (CN19) shown in *Figure 20*. The central pin of CN19 must be positive.

Figure 20. Power supply connector CN19 (Front view)



7.16 ST-LINK/V2-1 programming connector CN20

The connector CN20 is used only for embedded ST-LINK/V2-1 programming during the board manufacturing. It is not populated by default and not for end user.

7.17 MFX programming connector CN21

The connector CN21 is used only for MFX (Multi-Function expander) programming during the board manufacturing. It is not populated by default and not for end user.

7.18 ST-LINK/V2-1 USB Micro-B connector CN22

The USB connector CN22 is used to connect the embedded ST-LINK/V2-1 to the PC to debug the board.

Figure 21. USB Micro-B connector (Front view)

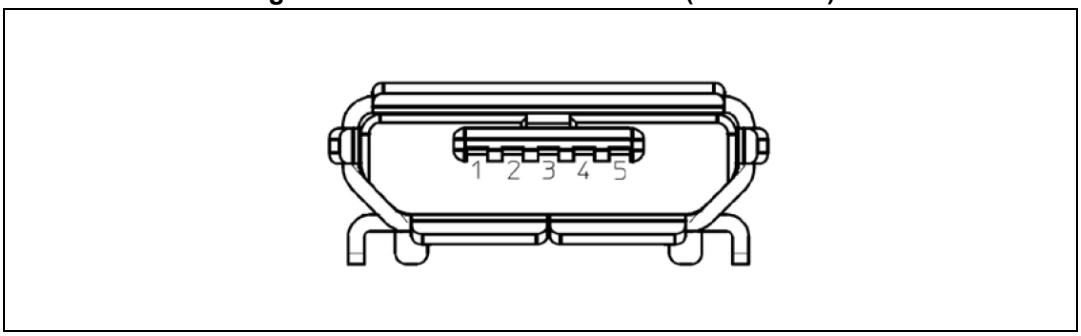


Table 34. USB Micro-B connector CN22

Pin number	Description	Pin number	Description
1	VBUS (power)	4	ID
2	DM	5	GND
3	DP	6,7,8,9,10,11	Shield

7.19 MEMS microphone coupon connectors CN24 and CN25

Figure 22. MEMS microphone coupon connectors CN24 and CN25 (Top view)

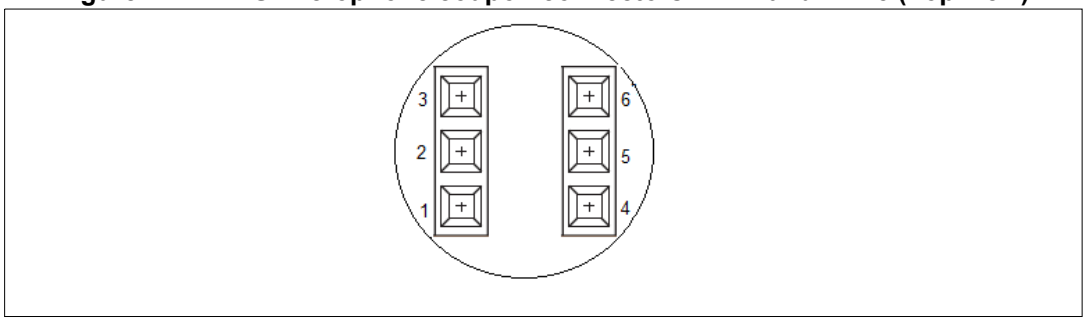


Table 35. MEMS microphone coupon connectors CN24 and CN25

Pin number	Description	Pin number	Description
1	DATA	4	VDD
2	GND	5	L/R
3	CLK	6	NC

7.20 CAN D-type 9-pin male connector CN26

Figure 23. CAN D-type 9-pin male connector (Front view)

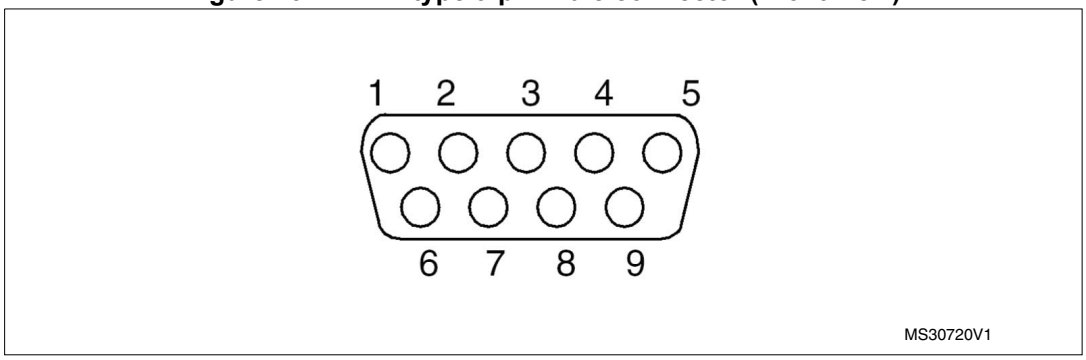


Table 36. CAN D-type 9-pin male connector CN26

Pin number	Description	Pin number	Description
1,4,8,9	NC	7	CANH
2	CANL	3,5,6	GND

7.21 Audio jack (speaker) CN27

A 3.5mm stereo audio jack CN27 for speaker out is available on the STM32F769I-EVAL evaluation board to support external speaker.

7.22 Audio jack CN28

A 3.5mm stereo audio jack CN28 is available on the STM32F769I-EVAL evaluation board to support headset (headphone and microphone integrated).

7.23 SPDIF IN connector CN29

Figure 24. SPDIF IN connector CN29 (Front view)

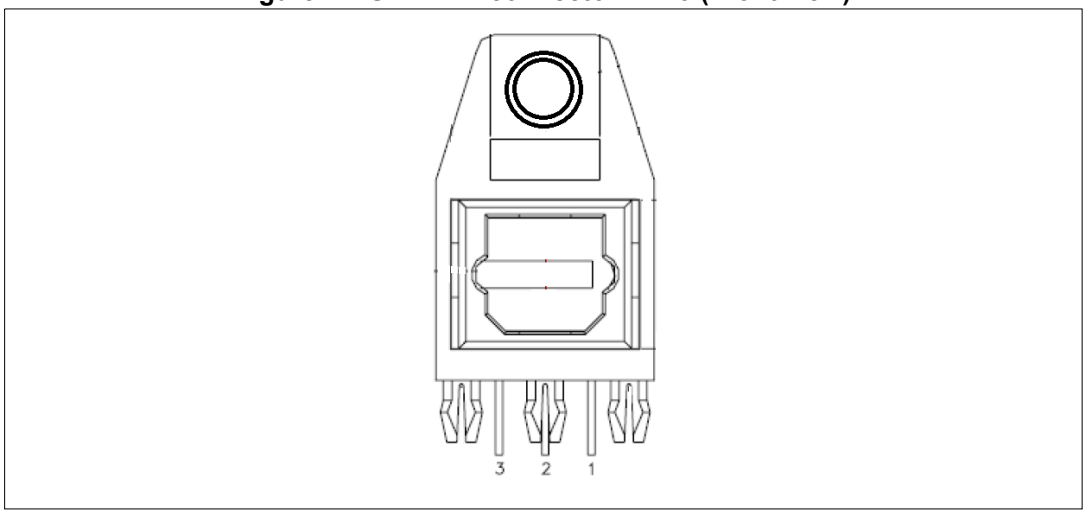


Table 37. SPDIF IN connector CN29

Pin number	Description	Pin number	Description
1	SPDIF_RX1(PG12)	3	VCC
2	GND	-	-

Appendix A STM32F769I-EVAL I/O assignment

Table 38. STM32F769I-EVAL I/O assignment

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
A1	PE4	A20/TRACED1	-	-
A2	PE3	A19/TRACED0	-	-
A3	PE2	A23/TRACECLK/MII_TXD3	-	-
A4	PG14	MII_TXD1	-	-
A5	PE1	NBL1	-	-
A6	PE0	NBL0	-	-
A7	PB8	Audio and EXPANDER and ACP and RF_I2C1_SCL	-	-
A8	PB5	ULPI_D7/LCD_G7	-	-
A9	PB4	NJTRST/SD2_D3	-	-
A10	PB3	JTDO/SD2_D2	-	-
A11	PD7	SD2_CMD	-	-
A12	PC12	SD1_CK	-	D9
A13	PA15	JTDI	-	-
A14	PA14	JTCK-SWCLK	-	-
A15	PA13	JTMS-SWDIO	-	-
B1	PE5	A21/TRACED2/LCD_G0	-	D6
B2	PE6	A22/SAI2_MCLK_B/TRACED3/LCD_G1	-	D7
B3	PG13	MII_TXD0	-	-
B4	PB9	Audio and EXPANDER and ACP and RF_I2C1_SDA	-	-
B5	PB7	-	-	VSYNC
B6	PB6	QSPI_BK1_NCS/CEC	-	-
B7	PG15	SDNCAS	-	-
B8	PG11	MII_TX_EN	NTC_BYPASS_IO	-
B9	PJ13	LCD_B1	-	-
B10	PJ12	LCD_B0	-	-
B11	PD6	DFSDM_DATA1/SD2_CLK	-	D10
B12	PD0	D2	-	-
B13	PC11	SD1_D3	-	D4
B14	PC10	SD1_D2//EXT_RESET	-	D8
B15	PA12	CAN1_TX/USB_FS1_DP	PFC_SYNC2_TIM1_ETR	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
C1	VBAT	VBAT	-	-
C2	PI8- ANTI TAMP2	EXPANDER_INT	-	-
C3	PI4	NBL2	-	-
C4	PK7	LCD_DE/DSI_RESET	-	-
C5	PK6	LCD_B7	-	-
C6	PK5	LCD_B6	-	-
C7	PG12	SPDIF_RX1	-	-
C8	PG10	SD2_D1	-	-
C9	PJ14	LCD_B2	-	-
C10	PD5	NWE	-	-
C11	PD3	DFSDM_CLK	-	D5
C12	PD1	D3	-	-
C13	PI3	D27	-	-
C14	PI2	D26	-	-
C15	PA11	CAN1_RX/USB_FS1_DM	PFC_PWM_TIM1_1_CH4	-
D1	PC13-ANTI_TAMP	KEY_ TAMP1_WKUP2	-	-
D2	PF0	A0	-	-
D3	PI5	NBL3	-	-
D4	PI7	D29	-	-
D5	PI10	D31/MII_RX_ER	-	-
D6	PI6	D28	-	-
D7	PK4	LCD_B5	-	-
D8	PK3	LCD_B4	-	-
D9	PG9	SAI2_FS_B/SD2_D0	-	-
D10	PJ15	LCD_B3	-	-
D11	PD4	NOE	-	-
D12	PD2	SD1_CMD	-	D11
D13	PH15	D23	-	-
D14	PI1	D25	-	-
D15	PA10	RS232_USART1_RX/USB_FS1_ID	-	-
E1	PC14-OSC32_IN	OSC32_IN	-	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
E2	PF1	A1	-	-
E3	PI12	LCD_HSYNC	-	-
E4	PI9	D30	-	-
E5	PDR_ON	-	-	-
E6	BOOT	BOOT	-	-
E7	VDD_3	-	-	-
E8	VDD_11	-	-	-
E9	VDD_10	-	-	-
E10	VDD_15	-	-	-
E11	VCAP2	-	-	-
E12	PH13	D21	-	-
E13	PH14	D22	-	-
E14	PI0	D24	-	-
E15	PA9	RS232_USART1_TX/ USB_FS1_VBUS	-	-
F1	PC15-OSC32_OUT	OSC32_OUT	-	-
F2	VSS_18	-	-	-
F2	VSS_13	-	-	-
F3	PI11	ULPI_DIR/LCD_G6	-	-
F4	VDD_13	-	-	-
F5	VDD_17	-	-	-
F6	VSS_3	-	-	-
F7	VSS_11	-	-	-
F8	VSS_10	-	-	-
F9	VSS_15	-	-	-
F10	VSS 2	-	-	-
F11	VDD_2	-	-	-
F12	PK1	-	-	-
F13	PK2	-	-	-
F14	PC9	SD1_D1/LCD_G3	-	D3
F15	PA8	Backlight_PWM_TIM1_CH1 /MII_MCO	PFC_SYNC1_TIM1_1_CH1	-
G1	PH0 - OSC_IN	OSC_IN	-	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
G2	PF2	A2	-	-
G3	PI13	LCD_VSYNC	-	-
G4	PI15	LCD_R0/LED0	-	-
G5	VDD_18	-	-	-
G6	VSS_17	-	-	-
G10	VSS_9	-	-	-
G11	VDDUSB	-	-	-
G12	PJ11	-	-	-
G13	PK0	-	-	-
G14	PC8	SD1_D0/NAND_NCE	WH_TIM8_CH3	D2
G15	PC7	FMC_NE1	VH_TIM8_CH2	D1
H1	PH1 - OSC_OUT	OSC_OUT	-	-
H2	PF3	A3	-	-
H3	PI14	LCD_CLK	-	-
H4	PH4	ULPI_NXT	-	-
H5	VDD_5	-	-	-
H6	VSS_5	-	-	-
H10	VSS_20	-	-	-
H11	VDD_20	-	-	-
H12	PJ8	-	-	-
H13	PJ10	-	-	-
H14	PG8	SDCLK/MII_PPS_OUT	-	-
H15	PC6	FMC_NWAIT	UH_TIM8_CH1	D0
J1	NRST	NRST	-	-
J2	PF4	A4	-	-
J3	PH5	SDNWE	-	-
J4	PH3	SDNE0/MII_COL	-	-
J5	VDD_12	-	-	-
J6	VSS_12	-	-	-
J10	VSS_8	-	-	-
J11	VDD_8	-	-	-
J12	PJ7	-	-	-
J13	PJ9	-	-	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
J14	PG7	NAND_INT	-	-
J15	PG6	FMC_NE3	-	-
K1	PF7	QSPI_BK1_IO2	-	-
K2	PF6	QSPI_BK1_IO3	-	-
K3	PF5	A5	-	-
K4	PH2	SDCKE0	-	-
K5	VDD_4	-	-	-
K6	VSS_4	-	-	-
K7	VSS_6	-	-	-
K8	VSS_7	-	-	-
K9	VSS_1	-	-	-
K10	VSS_14	-	-	-
K11	VDD_14	-	-	-
K12	PJ6	-	-	-
K13	PD15	D1	-	-
K14	PB13	ULPI_D6/USB_FS2_VBUS	-	-
K15	PD10	D15	-	-
L1	PF10	POT_ADC3_IN8	-	-
L2	PF9	QSPI_BK1_IO1	-	-
L3	PF8	QSPI_BK1_IO0	-	-
L4	PC3	MII_TX_CLK	CURRENT_C_ADC3_123_IN13	-
L5	BYPASS_REG	-	-	-
L6	VSS_19	-	-	-
L7	VDD_19	-	-	-
L8	VDD_6	-	-	-
L9	VDD_7	-	-	-
L10	VDD_1	-	-	-
L11	VCAP1	-	-	-
L12	PD14	D0	-	-
L13	PB12	ULPI_D5/USB_FS2_ID	-	-
L14	PD9	D14	-	-
L15	PD8	D13	-	-
M1	VSSA	-	-	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
M2	PC0	ULPI_STP	-	-
M3	PC1	SAI1_SD_A/MII_MDC	CURRENT_A_ADC1_123_IN11	-
M4	PC2	MII_TXD2	CURRENT_B_ADC2_123_IN12	-
M5	PB2	QSPI_CLK	-	-
M6	PF12	A6	-	-
M7	PG1	A11	-	-
M8	PF15	A9	-	-
M9	PJ4	LCD_R5	-	-
M10	PD12	A17	-	-
M11	PD13	A18	-	-
M12	PG3	A13	-	-
M13	PG2	A12	-	-
M14	PJ5	LCD_R6	-	-
M15	PH12	D20	-	-
N1	VREF-	-	-	-
N2	PA1	MII_RX_CLK	ENCODER_B_TIM5_5_CH2	-
N3	PA0-WKUP	SAI2_SD_B/MII_CRS	ENCODER_A_TIM5_5_CH1	-
N4	PA4	-	DAC_OUT1	HSYNC
N5	PC4	MII_RXD0	BUSVOLTAGE_ADC12_IN14	-
N6	PF13	A7	-	-
N7	PG0	A10	-	-
N8	PJ3	LCD_R4/LED3	-	-
N9	PE8	D5	-	-
N10	PD11	A16	-	-
N11	PG5	A15(BA1)	-	-
N12	PG4	A14(BA0)	-	-
N13	PH7	MII_RXD3	-	-
N14	PH9	D17	-	-
N15	PH11	D19	-	-
P1	VREF+	-	-	-
P2	PA2	SAI2_SCK_B/MII_MDIO	INDEX_TIM5_5_CH3	-
P3	PA6	-	STOP_TIM8_BKIN	PIXCLK
P4	PA5	ULPI_CK	DAC_OUT2	-
P5	PC5	MII_RXD1	HEATSINK_ADC12_IN15	-

Table 38. STM32F769I-EVAL I/O assignment (continued)

Pin No.	Pin Name	STM32F769I-EVAL standard	Motor control variant	Camera variant
P6	PF14	A8	-	-
P7	PJ2	LCD_R3/DSI_TE	-	-
P8	PF11	SDNRAS	-	-
P9	PE9	D6	-	-
P10	PE11	D8	-	-
P11	PE14	D11	-	-
P12	PB10	ULPI_D3	-	-
P13	PH6	MII_RXD2	DISSIPATIVE_BRAKE_TIM2_12_CH1	-
P14	PH8	D16	-	-
P15	PH10	D18	-	-
R1	VDDA	-	-	-
R2	PA3	ULPI_D0	-	-
R3	PA7	MII_RX_DV	UL_TIM8_CH1N	-
R4	PB1	ULPI_D2	WL_TIM8_CH3N	-
R5	PB0	ULPI_D1	VL_TIM8_CH2N	-
R6	PJ0	LCD_R1/LED1	-	-
R7	PJ1	LCD_R2/LED2	-	-
R8	PE7	D4	-	-
R9	PE10	D7	-	-
R10	PE12	D9	-	-
R11	PE15	D12	-	-
R12	PE13	D10	-	-
R13	PB11	ULPI_D4	-	-
R14	PB14	USB_FS2_DM	-	-
R15	PB15	USB_FS2_DP	-	-

Appendix B Schematics

This section provides design schematics for the STM32F769I-EVAL key features to help users to implement these features in application designs.

This section includes:

- Overall schematics for the board, see *Figure 25*
- MCU connections, see *Figure 26*
- Power supply, see *Figure 27*
- SRAM, Flash, SDRAM, see *Figure 28*
- Audio amplifier, see *Figure 29*
- LCD, camera and connector, see *Figure 30*
- Ethernet, see *Figure 31*
- USB OTG HS, see *Figure 32*
- USB OTG FS, see *Figure 33*
- RS-232, see *Figure 34*
- CAN and Quad-SPI, see *Figure 35*
- Peripherals, see *Figure 36*
- Motor control, *Figure 37*
- Extension connectors, see *Figure 38*
- ST-LINK/V2-1, see *Figure 39*
- MFX and LEDs, see *Figure 40*
- SWD and JTAG debuggers, see *Figure 41*
- MB1166 LCD board schematics, see *Figure 42*
- MB1183 camera module schematics, see *Figure 43*

Figure 25. STM32F769I-EVAL evaluation board

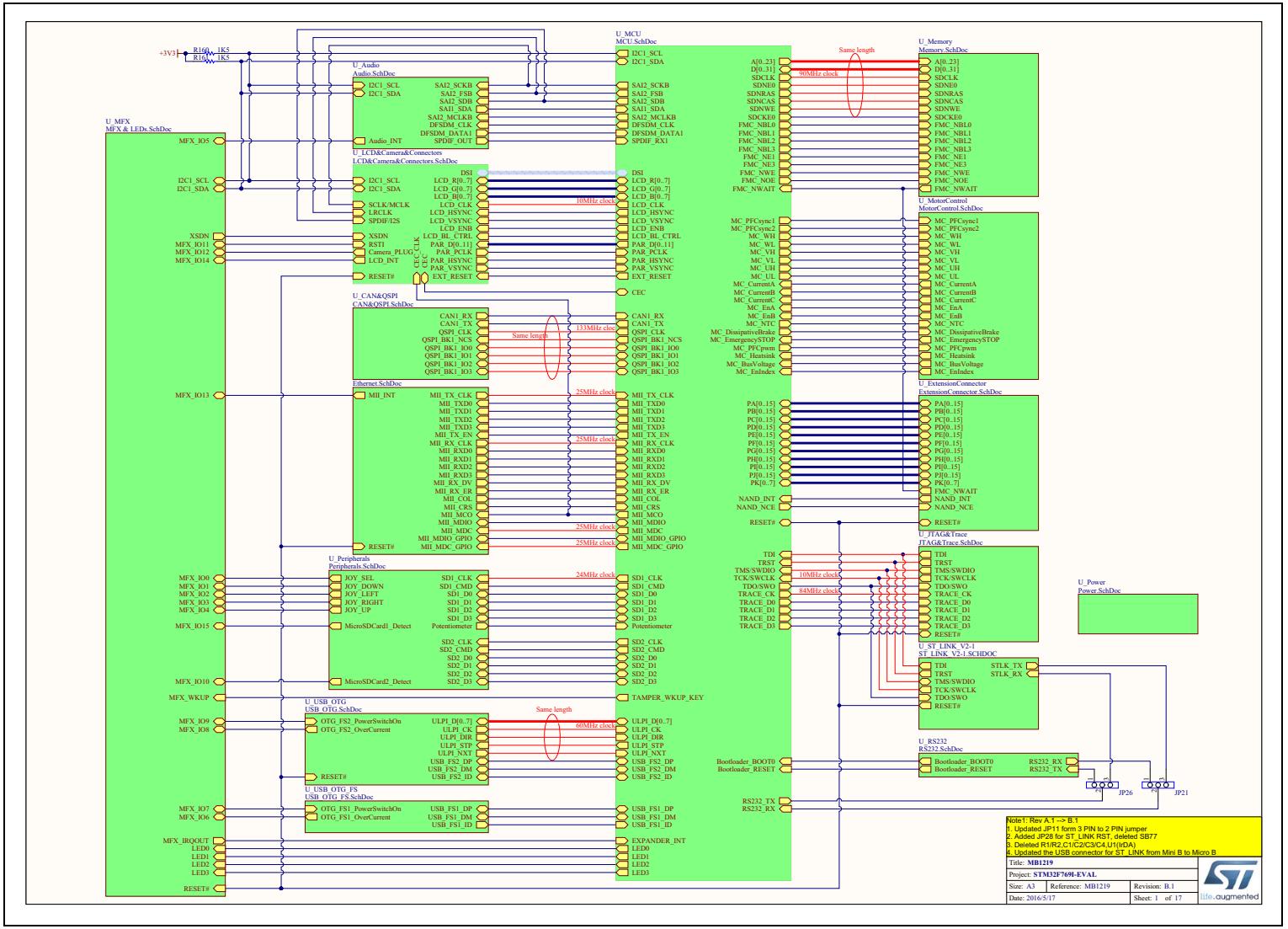


Figure 26. STM32F769I-EVAL MCU

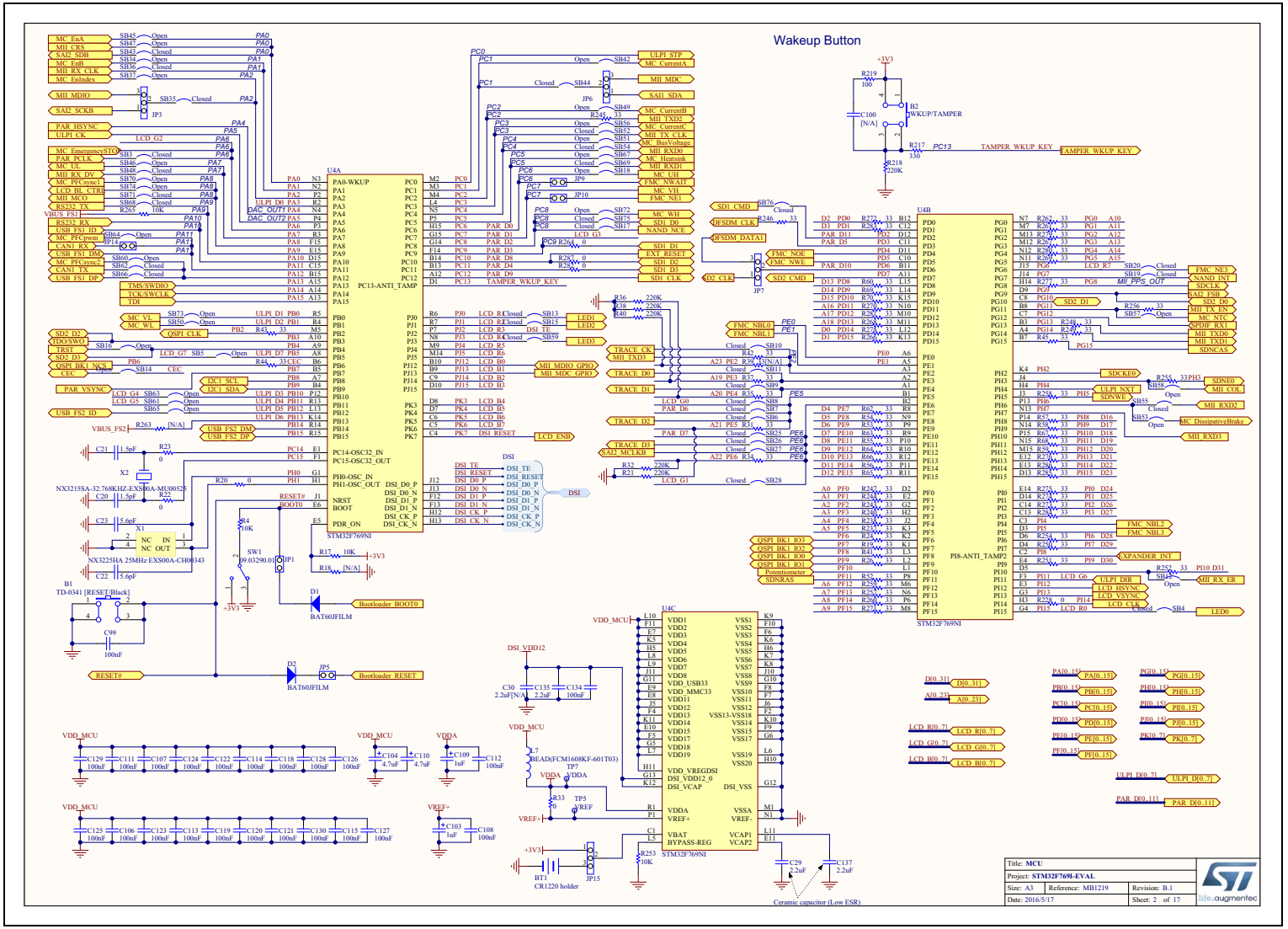


Figure 27. STM32F769I-EVAL Power

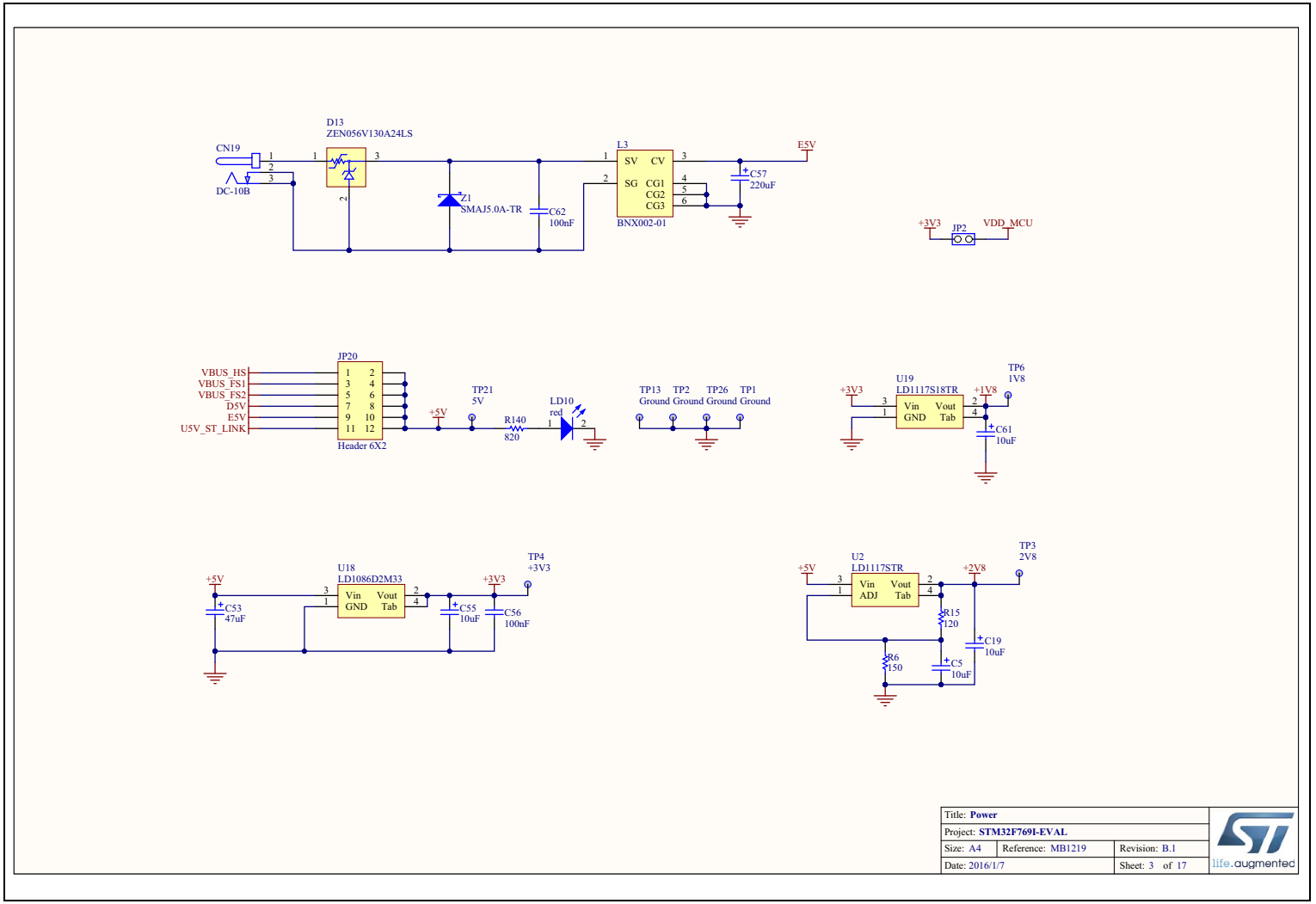


Figure 28. STM32F769I-EVAL SRAM, FLASH, SDRAM

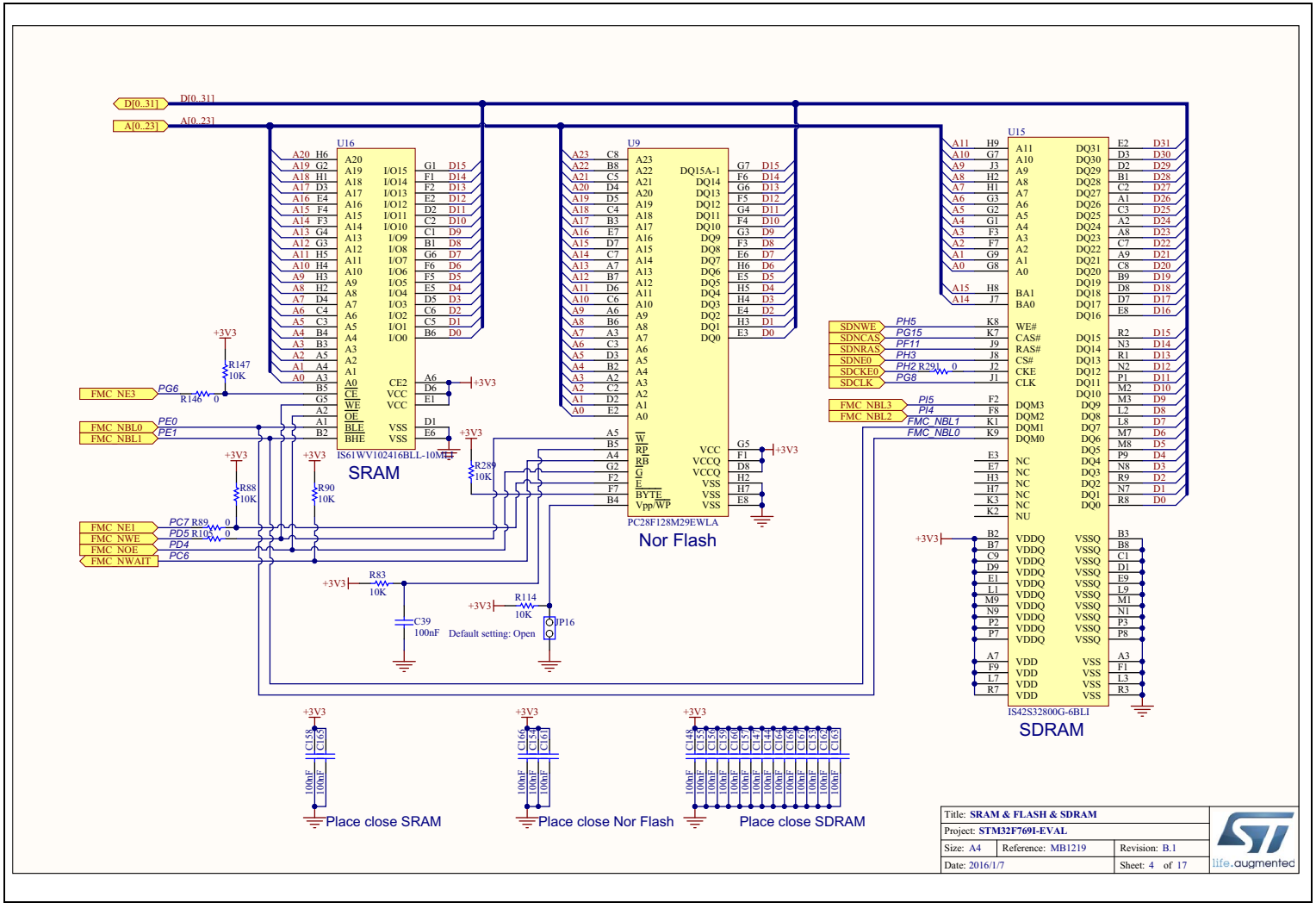


Figure 29. STM32F769I-EVAL Audio

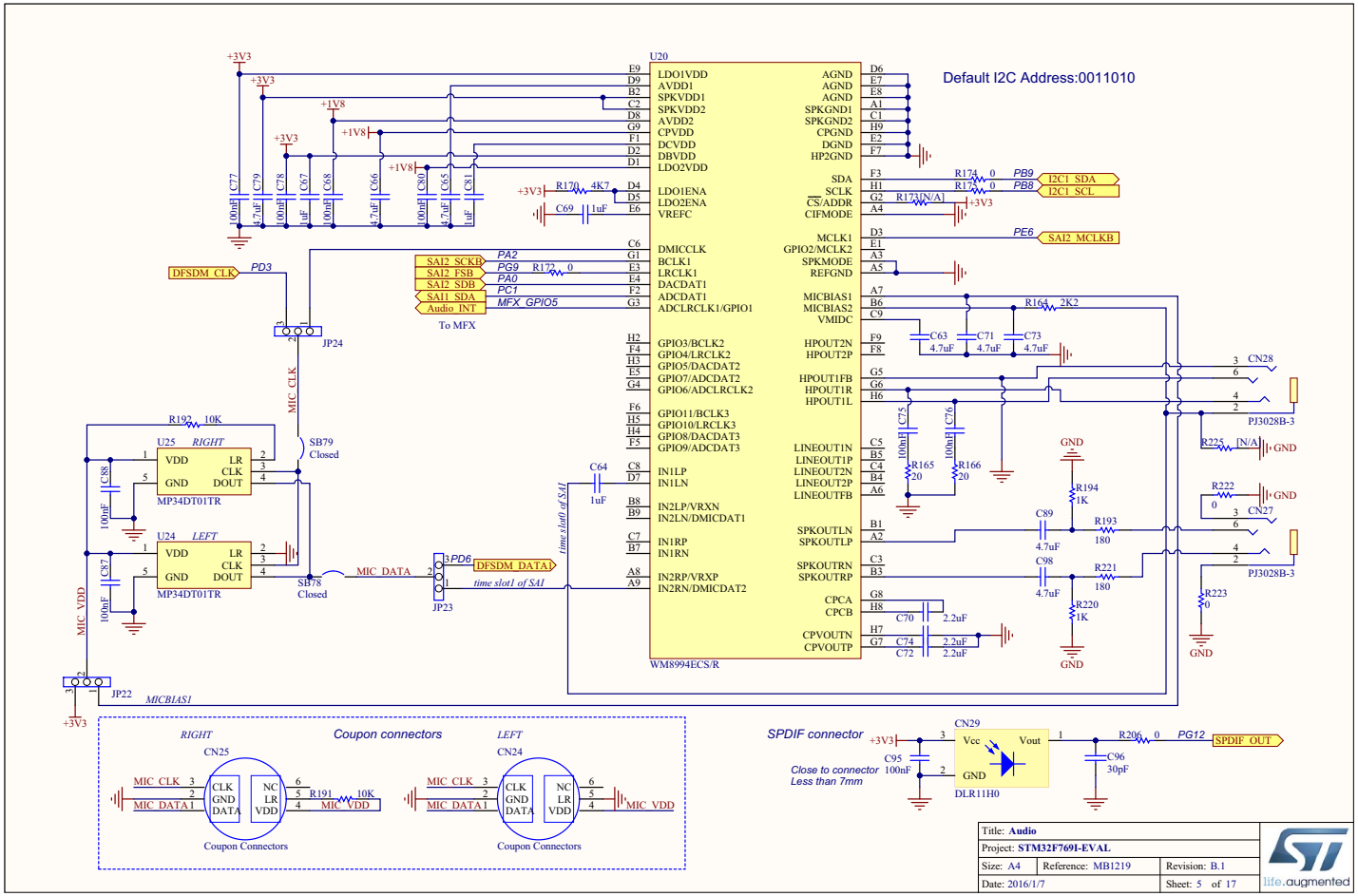


Figure 30. STM32F769I-EVAL LCD, camera, connector

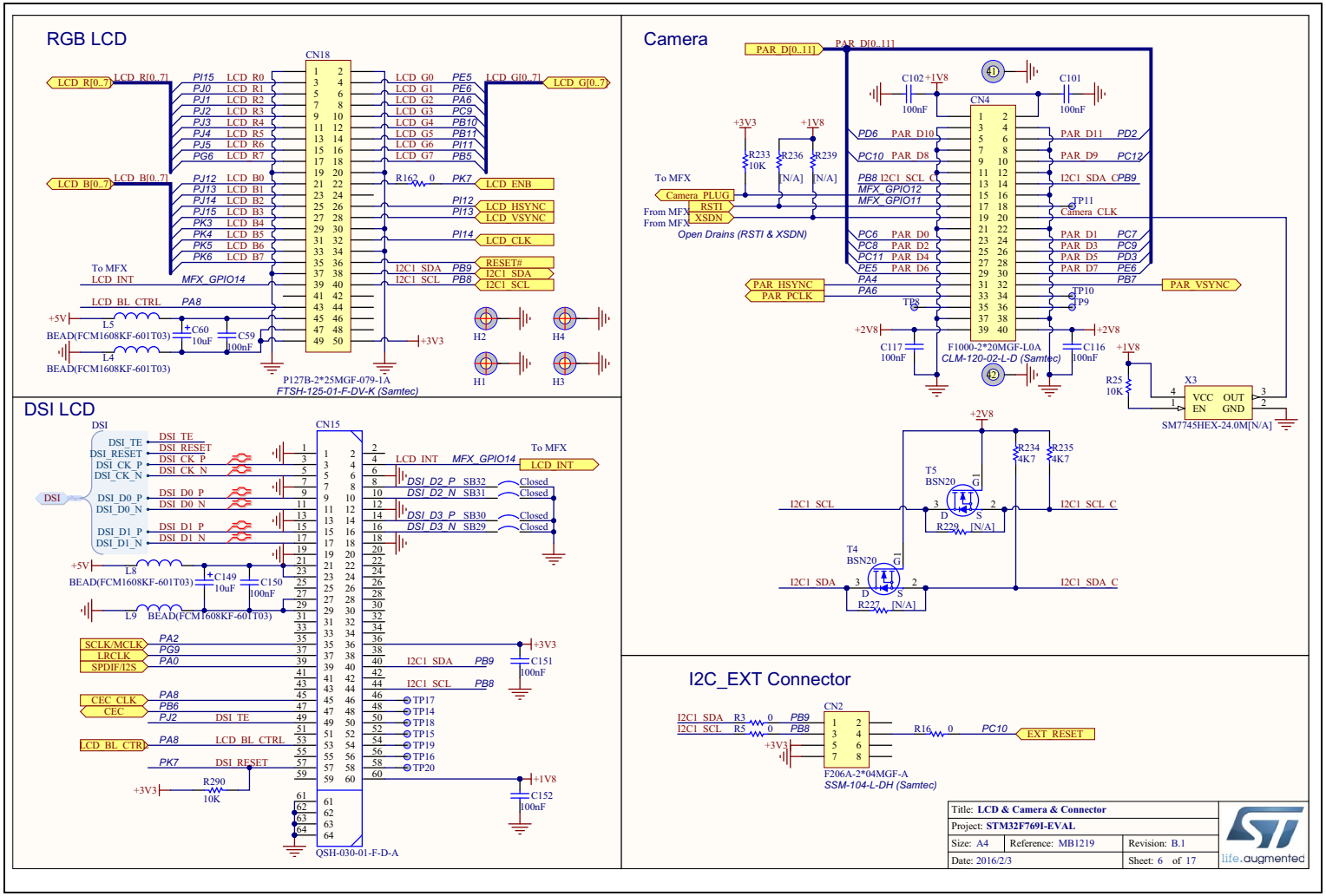


Figure 31. STM32F769I-EVAL Ethernet

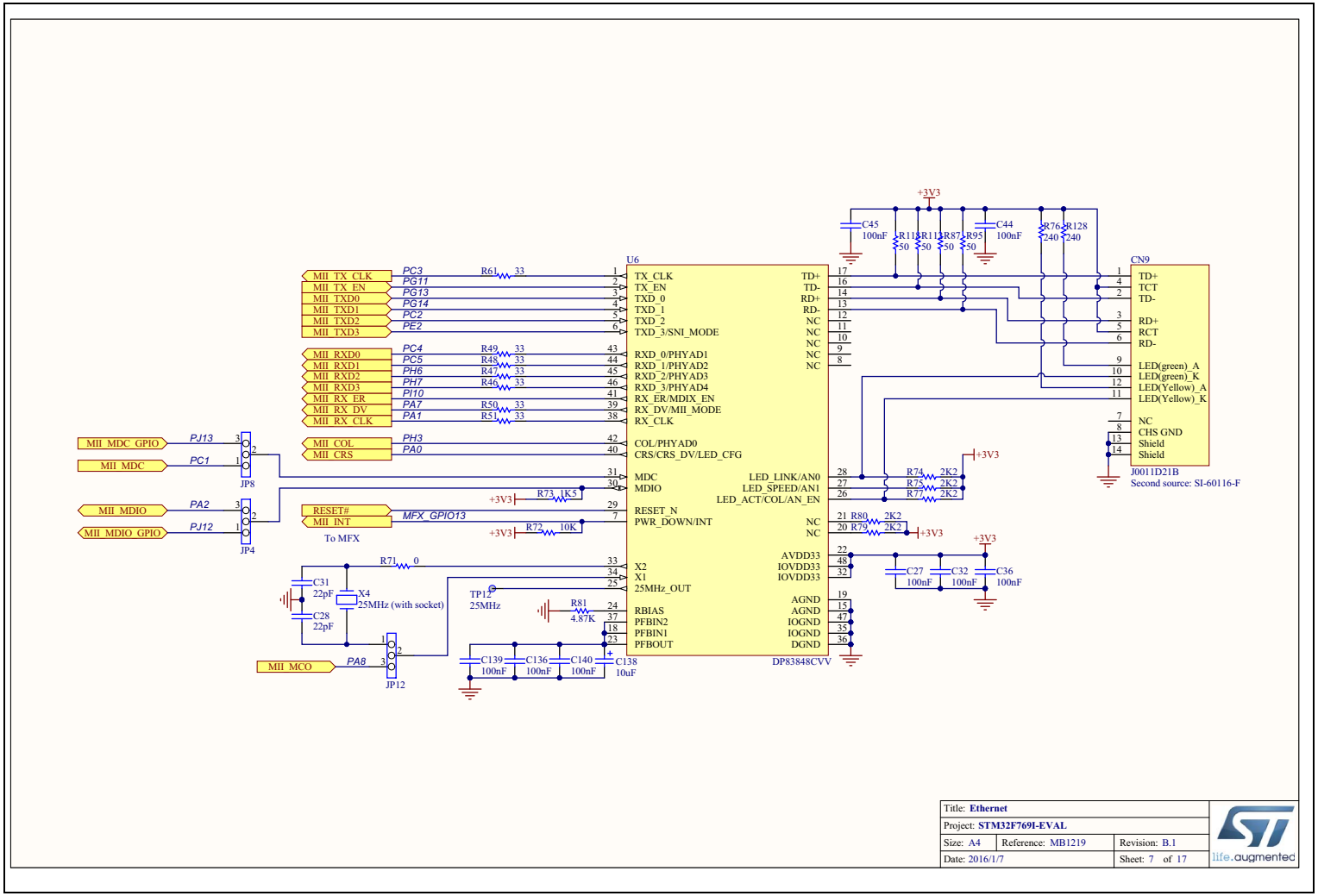


Figure 32. STM32F769I-EVAL USB OTG HS

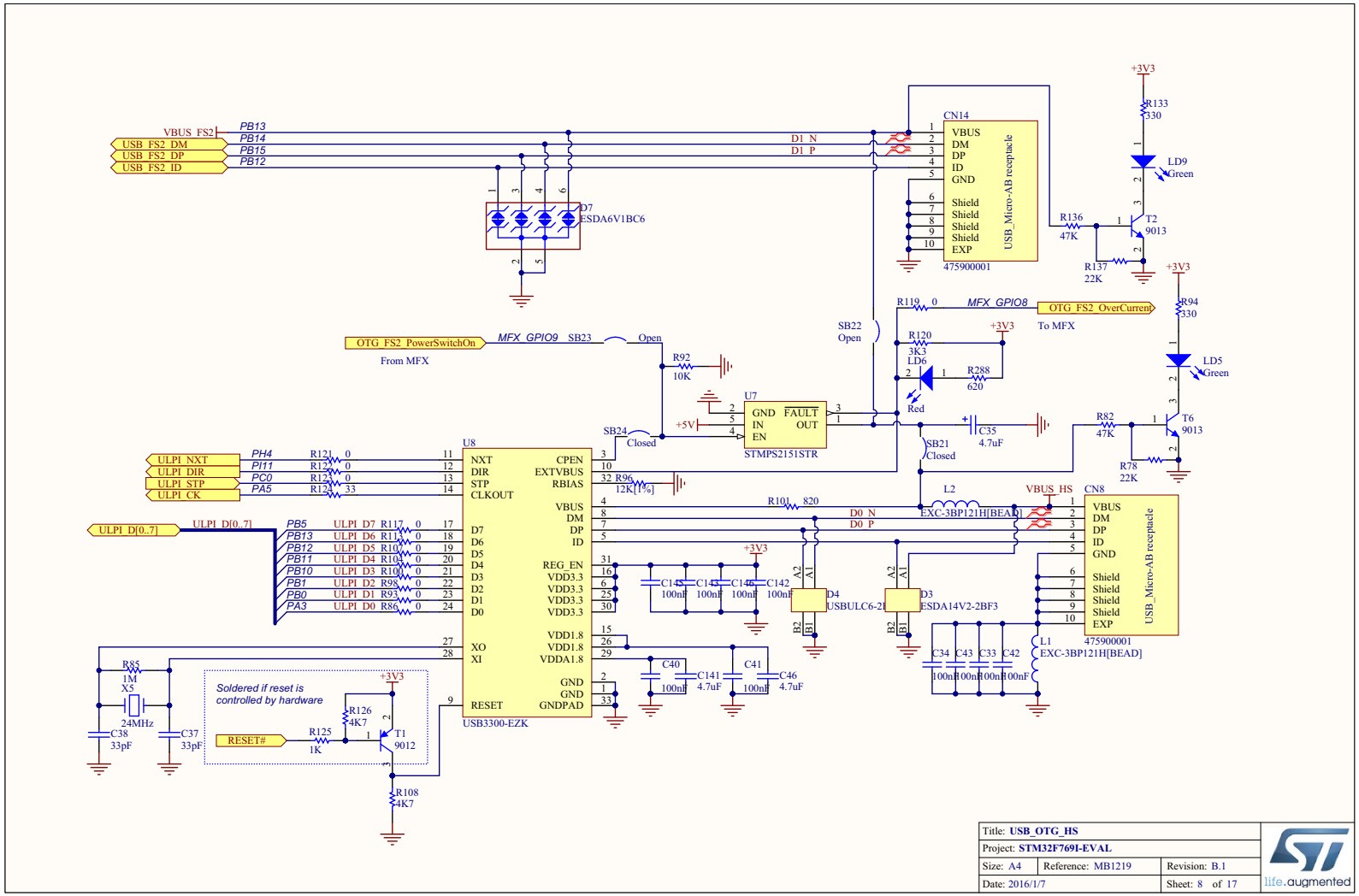


Figure 33. STM32F769I-EVAL USB OTG FS

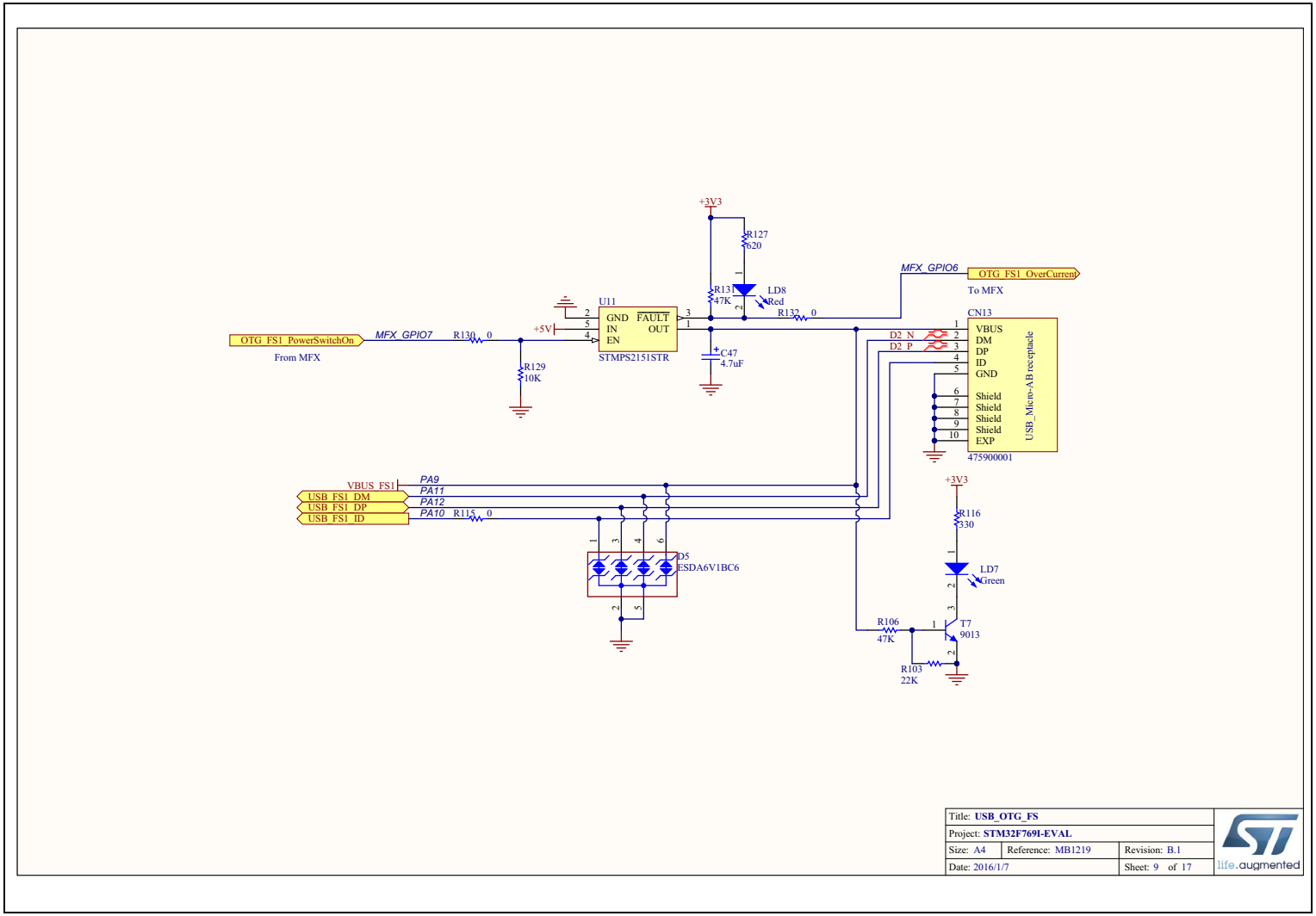


Figure 34. STM32F769I-EVAL RS-232

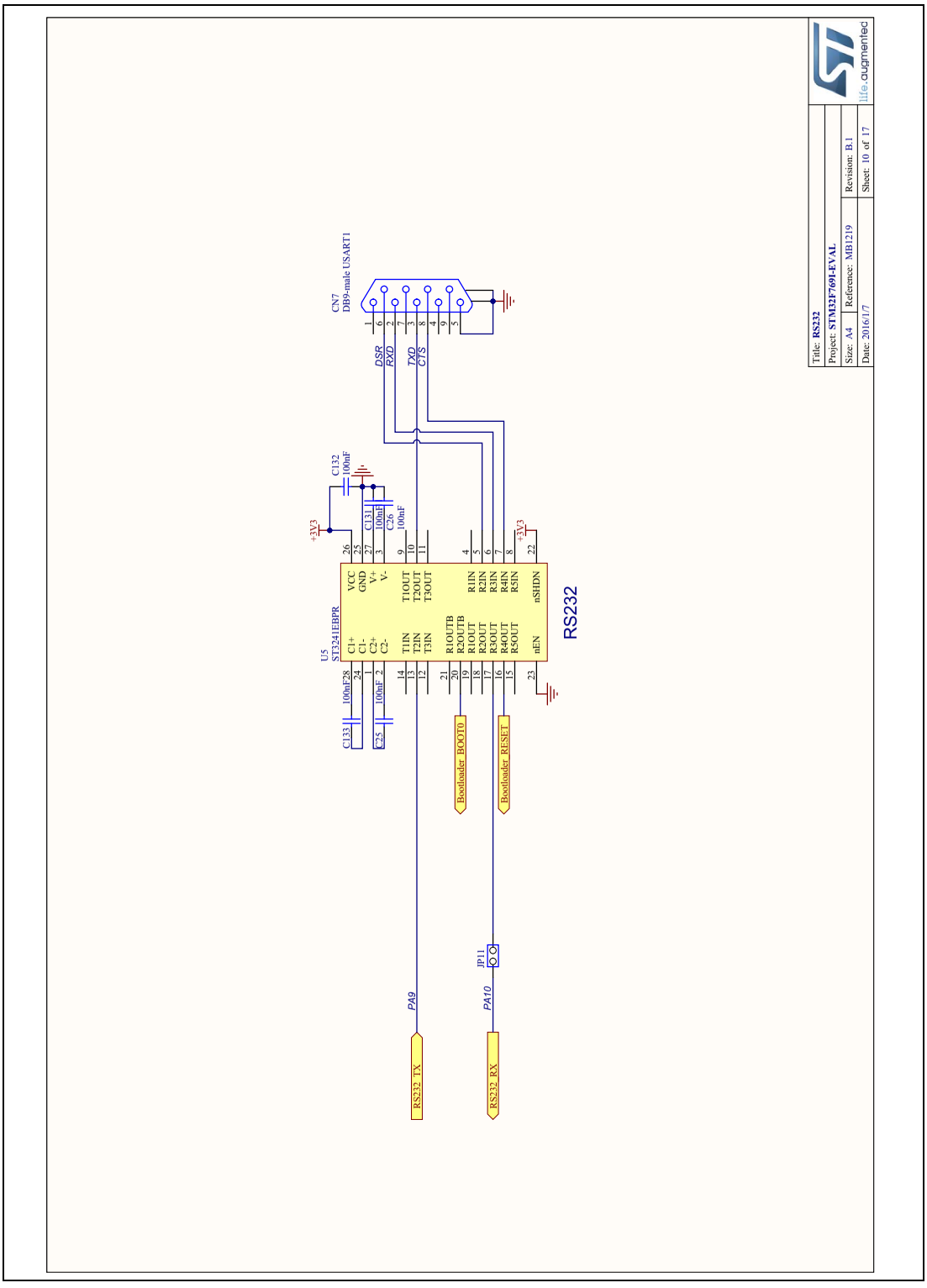


Figure 35. STM32F769I-EVAL CAN and Quad-SPI

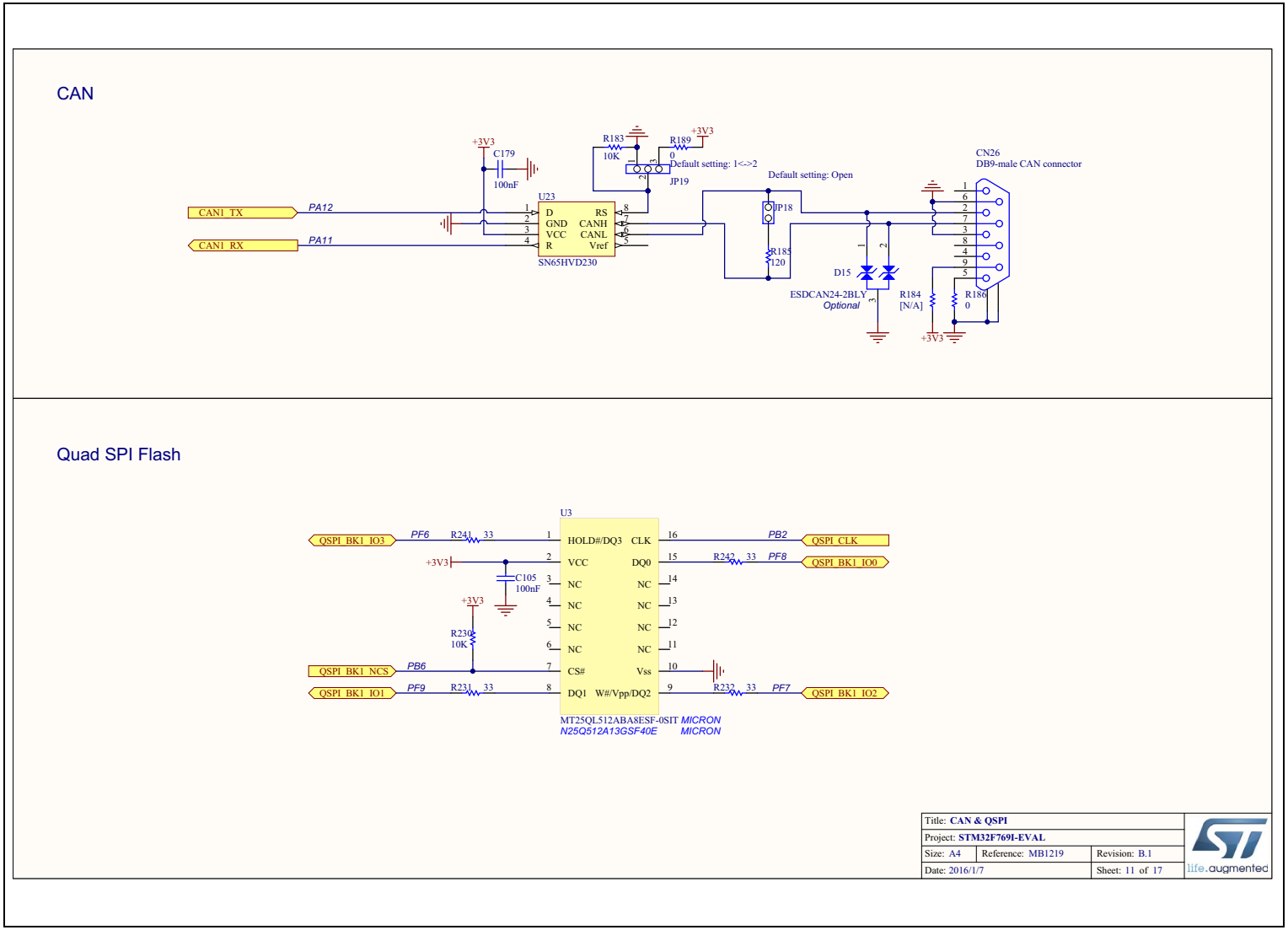


Figure 36. STM32F769I-EVAL Peripherals

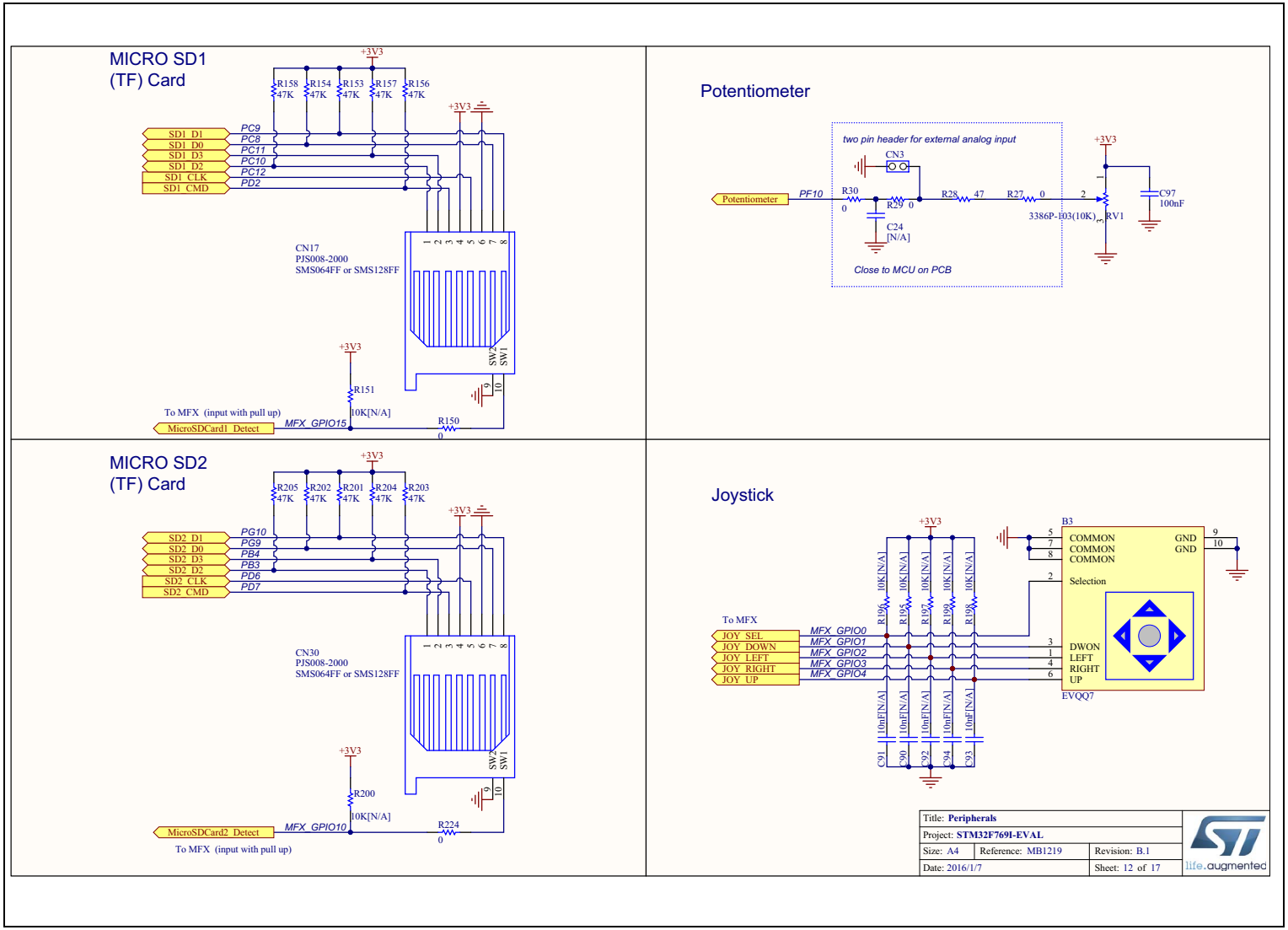


Figure 37. STM32F769I-EVAL motor control

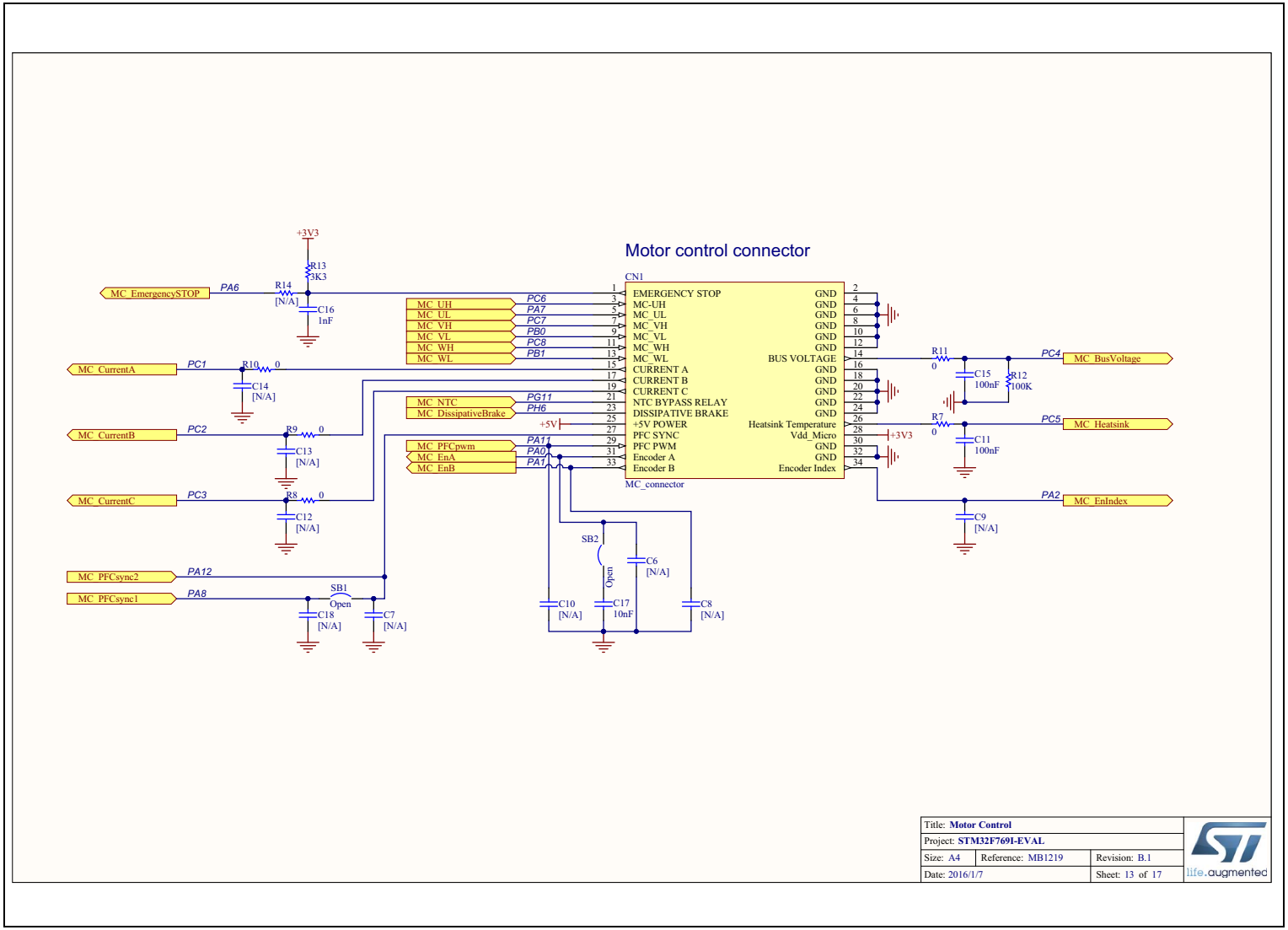


Figure 38. STM32F769I-EVAL extension connectors

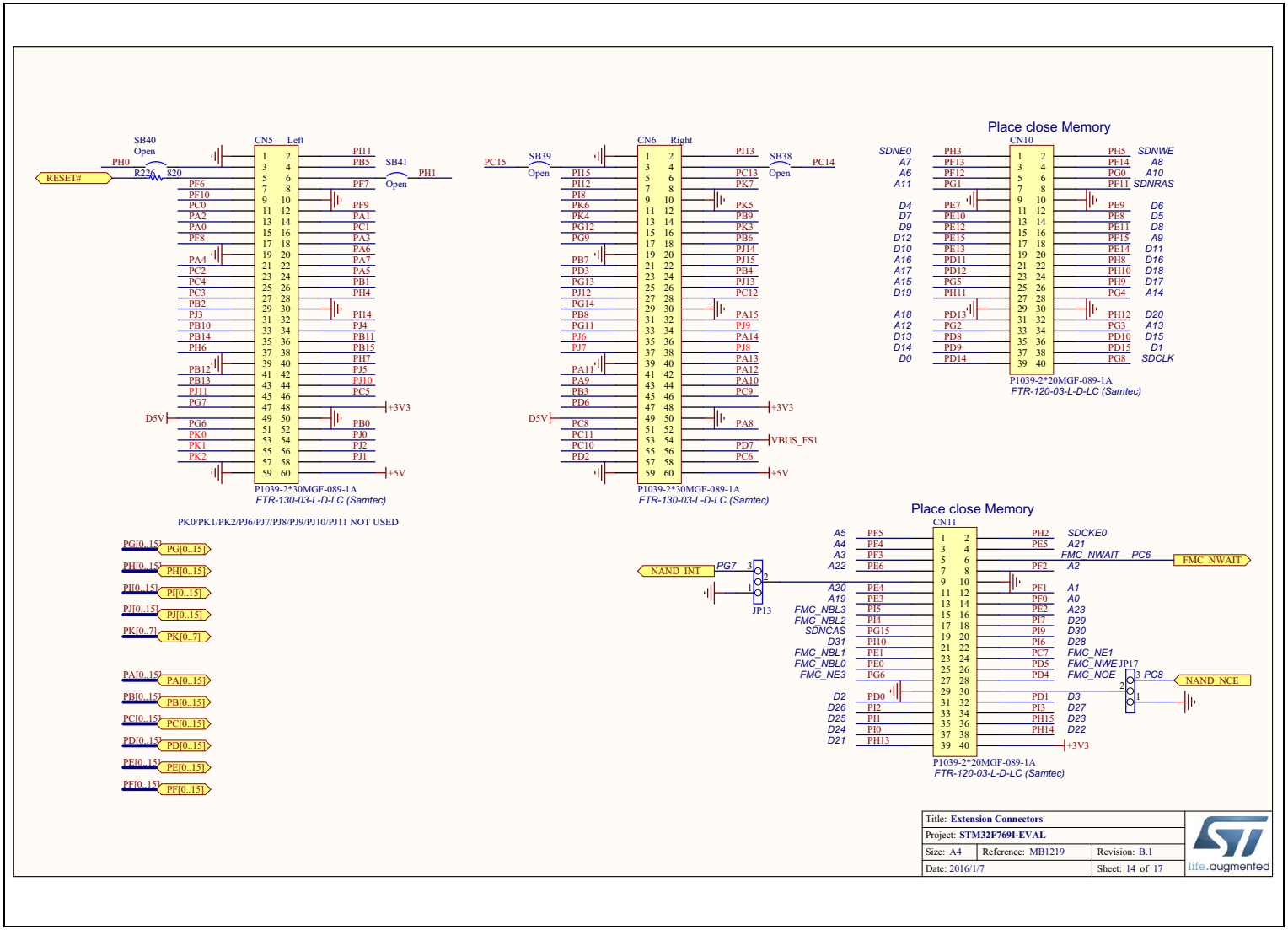


Figure 39. STM32F769I-EVAL ST-LINK/V2-1

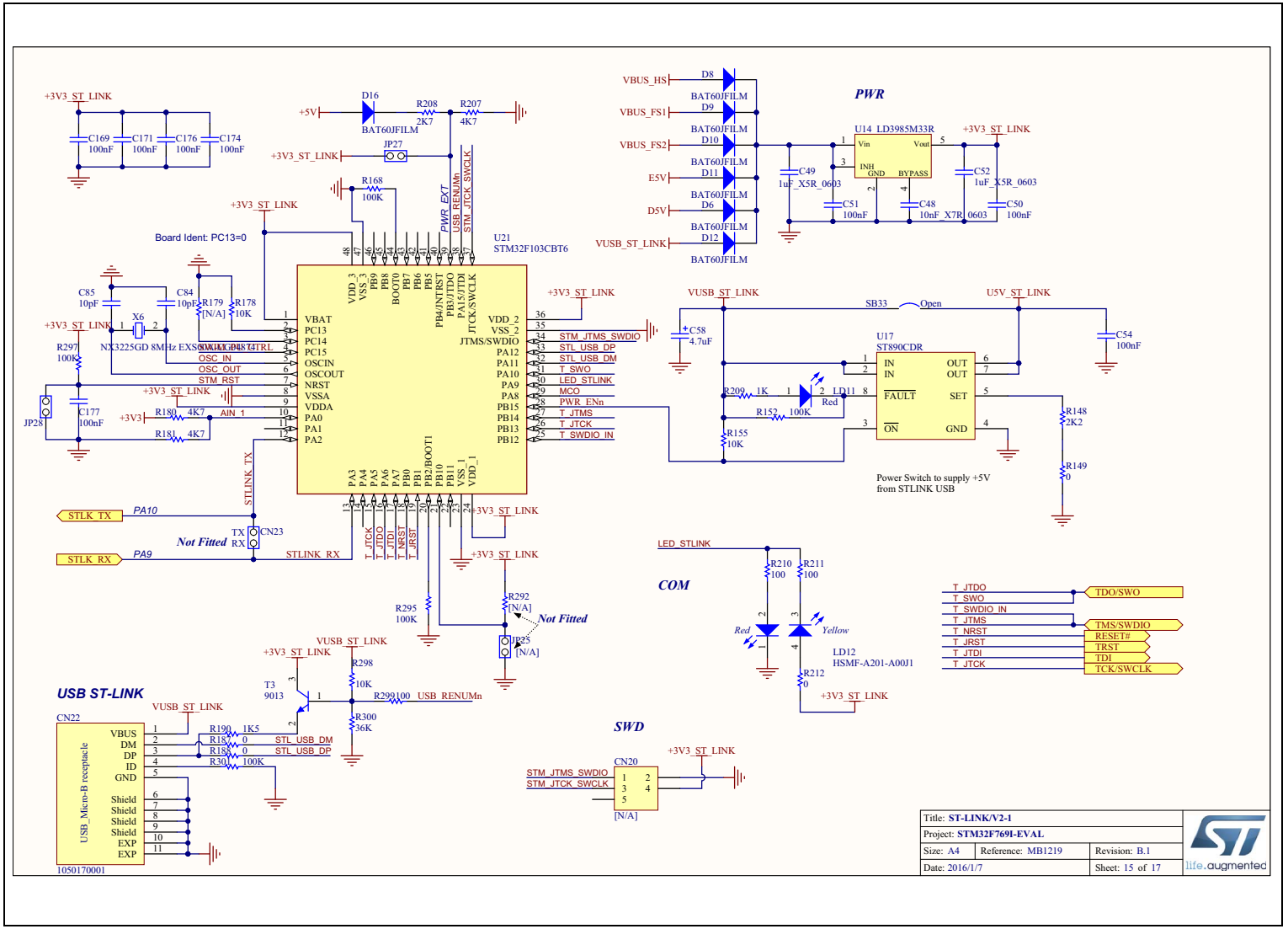


Figure 40. STM32F769I-EVAL MFX and LEDs

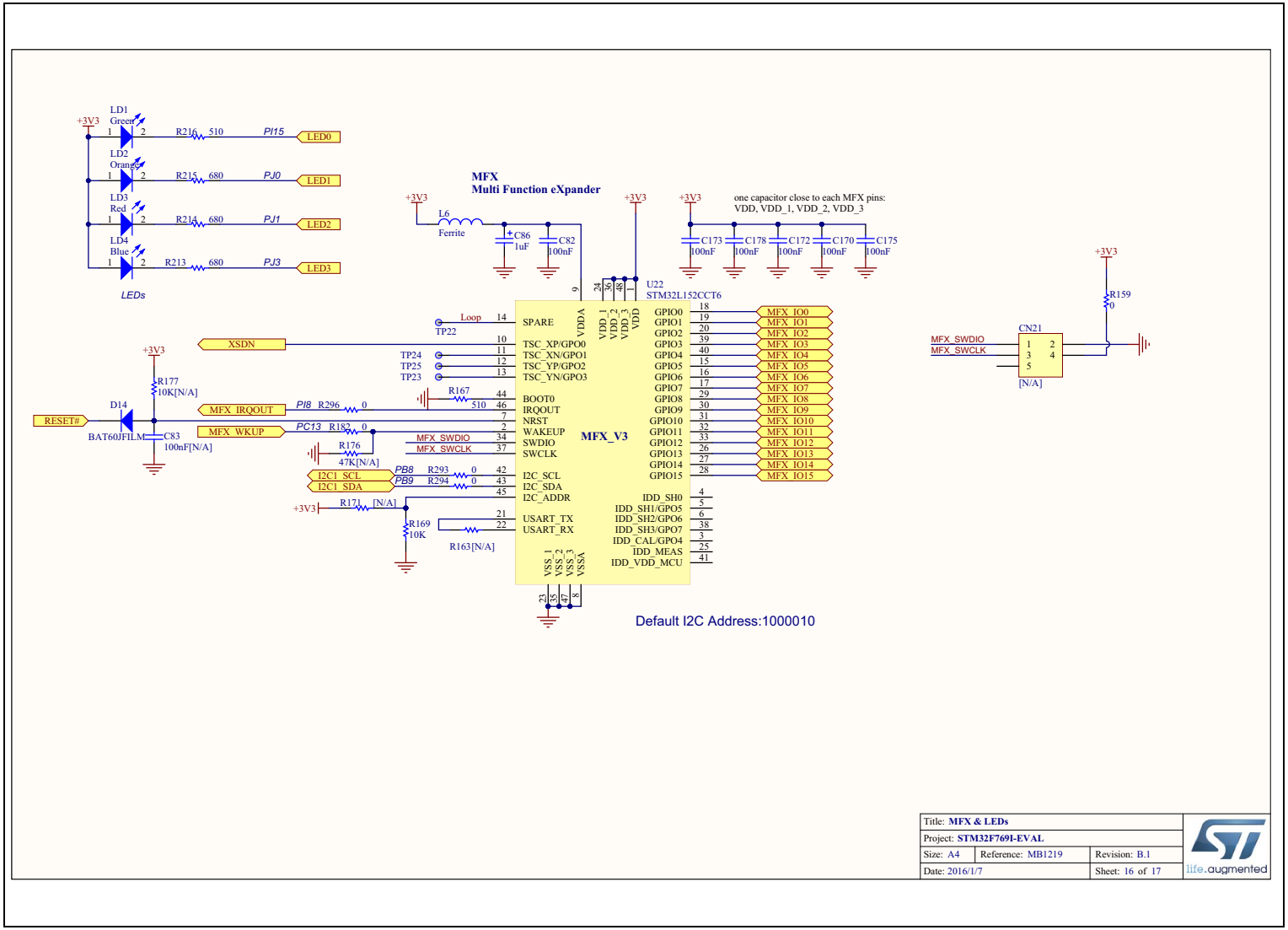


Figure 41. STM32F769I-EVAL JTAG and trace

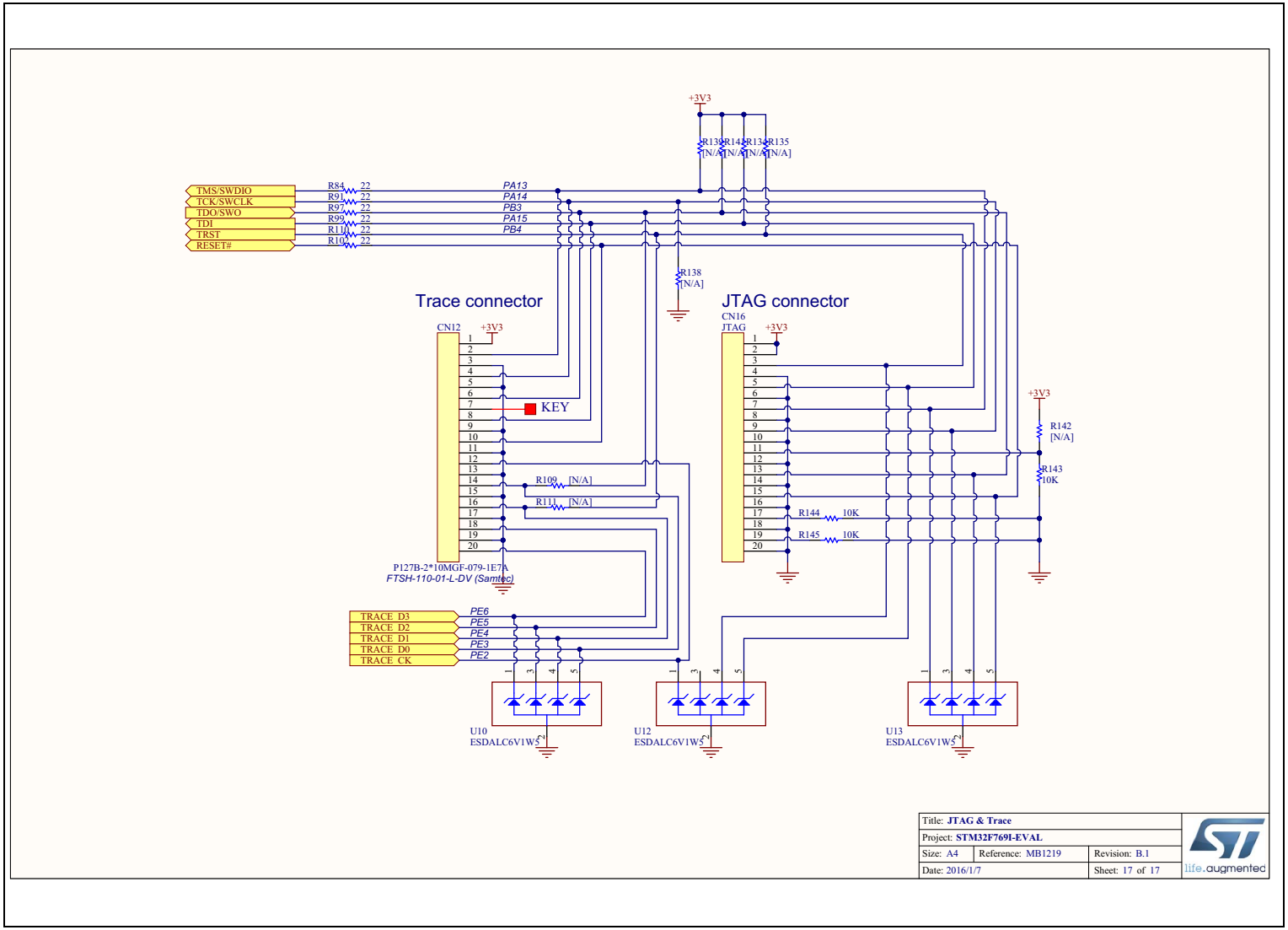


Figure 42. STM32F769I-EVAL 4-inch DSI LCD board

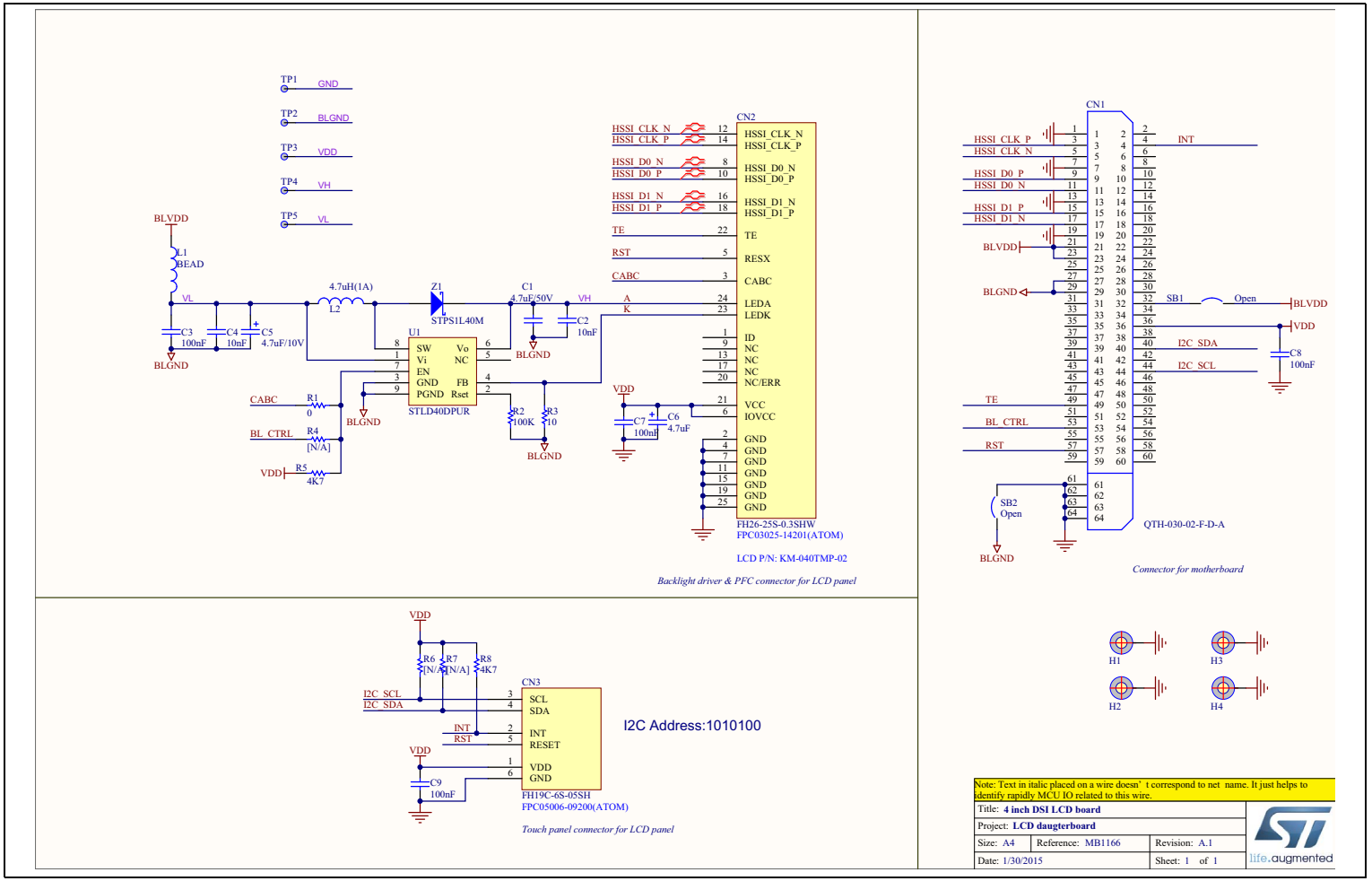
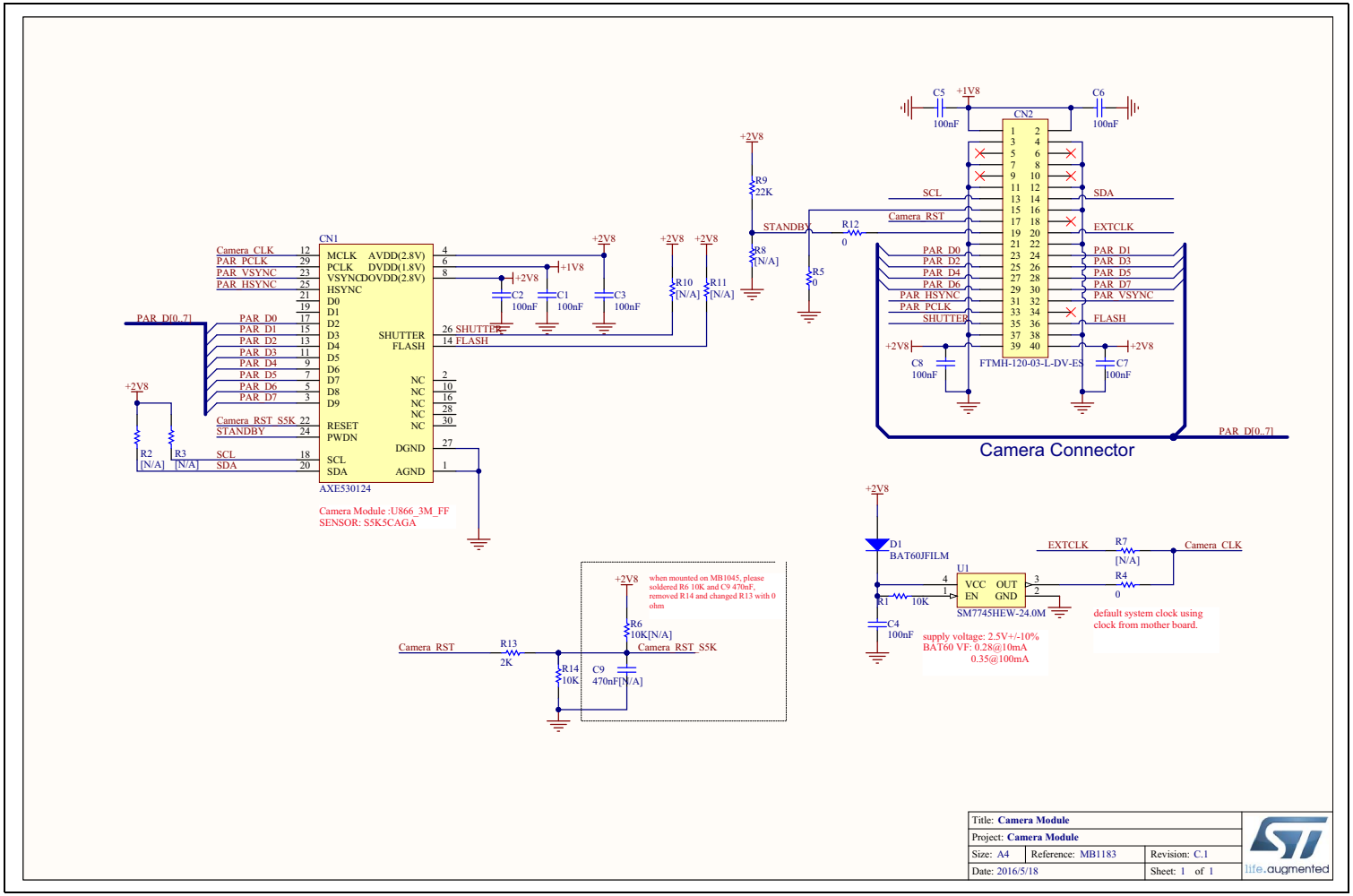


Figure 43. STM32F769I-EVAL camera module



Appendix C Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements

C.1 FCC Compliance Statement

C.1.1 Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

C.1.2 Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

C.1.3 Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

C.2 IC Compliance Statement

C.2.1 Compliance Statement

Industry Canada ICES-003 Compliance Label: CAN ICES-3 (A)/NMB-3(A).

C.2.2 Déclaration de conformité

Étiquette de conformité à la NMB-003 d'Industrie Canada : CAN ICES-3 (A)/NMB-3(A).

Appendix D CISPR32

D.1 Warning

Warning: This device is compliant with Class A of CISPR32. In a residential environment, this equipment may cause radio interference.

Revision history

Table 39. Document revision history

Date	Revision	Changes
23-May-2016	1	Initial release.
01-Dec-2016	2	Added sections: *Section Appendix C: Federal Communications Commission (FCC) and Industry Canada (IC) Compliance Statements*, *Section Appendix D: CISPR32*.
08-Mar-2017	3	Added boot loader note in *Section 6.5: Boot option* and ESD protection note in *Section 6.7: USB OTG1 FS*.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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