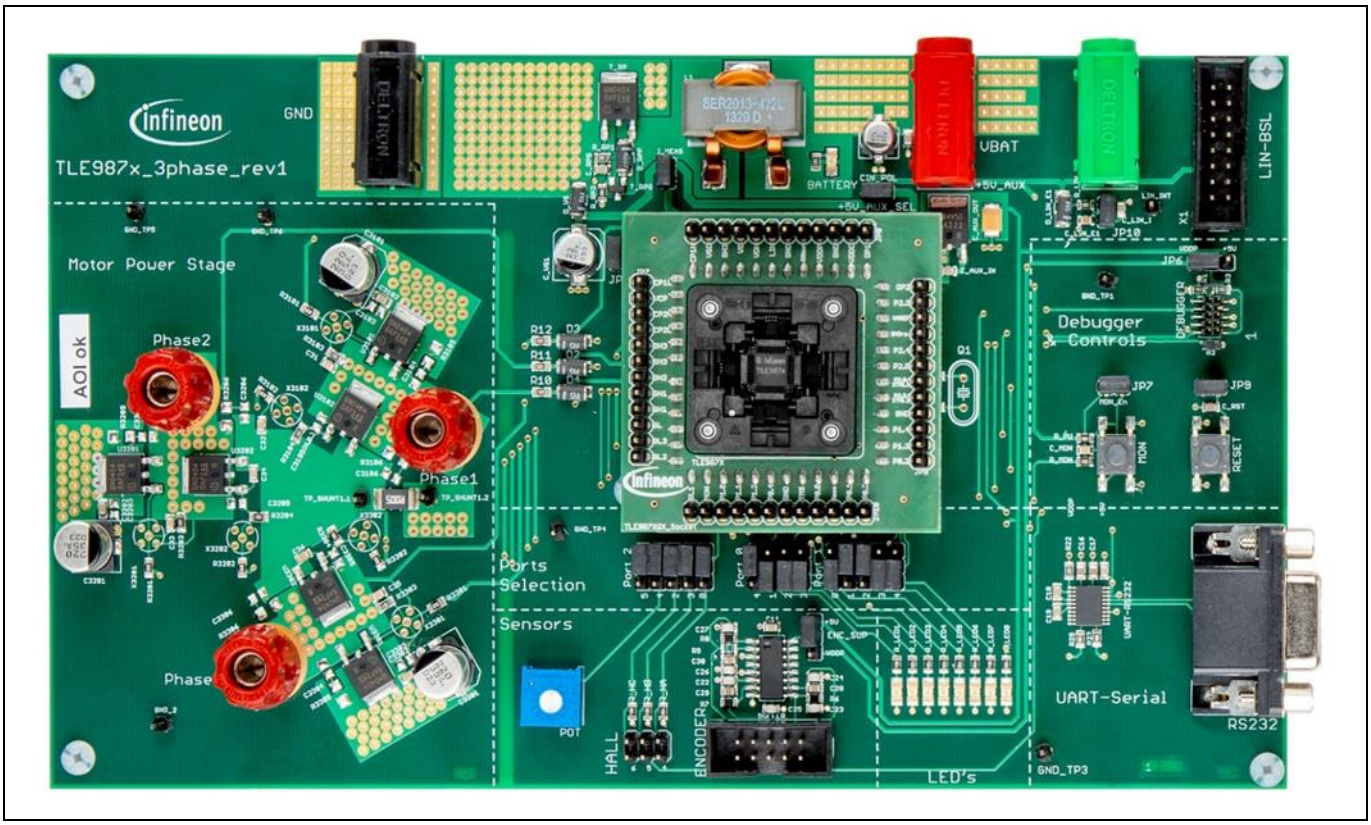
TLE987x EvalBoard Rev1.2 User Manual



About this document

Scope and purpose

This user manual is intented to help users using the TLE987x Evalboard. This Evalboard is designed to evaluate hardware and software functionalities of the TLE987x device family.

This manual provides additional information about the board's layout, jumper settings, interface and debug options. It introduces the evaluation platform as well as how to write software and download it to the TLE987x.

Intended audience

This document is for everyone who works with the TLE987x Evalboard.

About this document

Abbreviations and definitions

Table 1 Abbreviations

Abbreviation	Definition
BLDC	Brushless direct current
BSL	Bootstrap loader
GH1, 2, 3	Gate high-side MOSFETs for phases 1, 2
GL1, 2, 3	Gate low-side MOSFETs for phase 1, 2
GPIO	General purpose input / output
ISP	In-system programmer
LIN	Local interconnect network
MON	Monitor
n.c.	Not connected
n/u	Not used
OP1	Negative operational amplifier input
OP2	Positive operational amplifier input
RST	Reset
SL	Source low-side MOSFET
SWD	Arm® serial wire debug
TMS	Test mode select
UART	Universal asynchronous receiver transmitter
VAREF	Reference voltage
VBAT	Battery voltage supply
VCOM	Virtual COM-port
VCP	Voltage charge pump
VDDC	Core supply
VDDEXT	External voltage supply output
VDDP	I/O port supply
VDH	Voltage drain high-side MOSFET
VS	Battery supply input
VSD	Battery supply input for MOSFET driver

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1 Concept

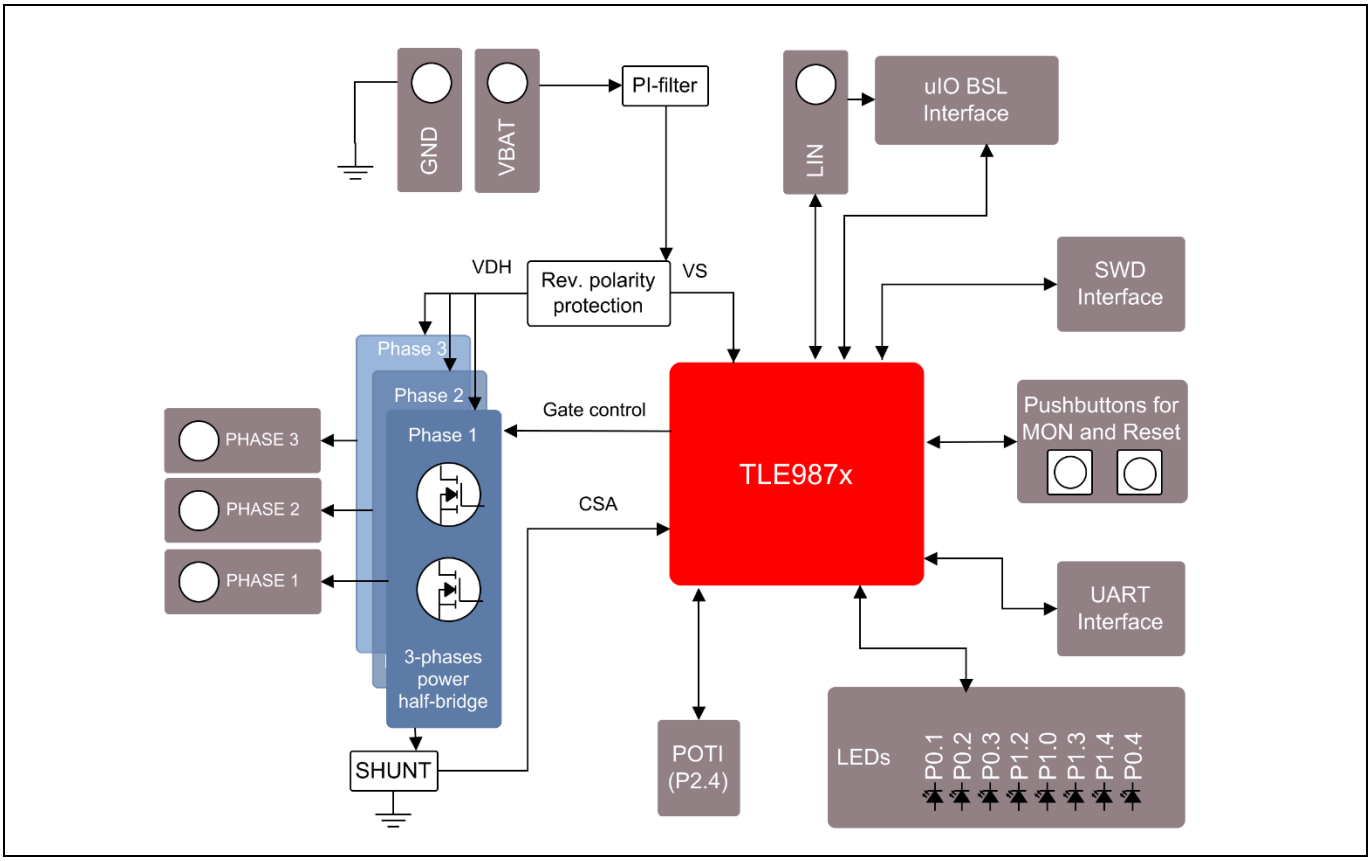

Figure 1 Board concept

This board is designed to provide a simple, easy-to-use tool for getting familiar with Infineon's Embedded Power IC TLE987x devices. A socket provides the possibility to test and evaluate all ICs of the TLE987x family. Every pin of the IC is connectable via rows of pin headers. The board is protected against reverse polarity of input voltage supply.

Three MOSFET half bridges are assembled on the board to drive a BLDC motor. The board is ready to be connected to a car supply or similar and offers a SWD port to connect an external debugger.

The evaluation board can be operated by standard laboratory equipment as power supply and LIN communication are working via banana jacks.

There is a battery LED that indicates that the board is connected to supply in the correct way. Otherwise reverse polarity protection secures the board from damage by cross connection.

2 Interconnects

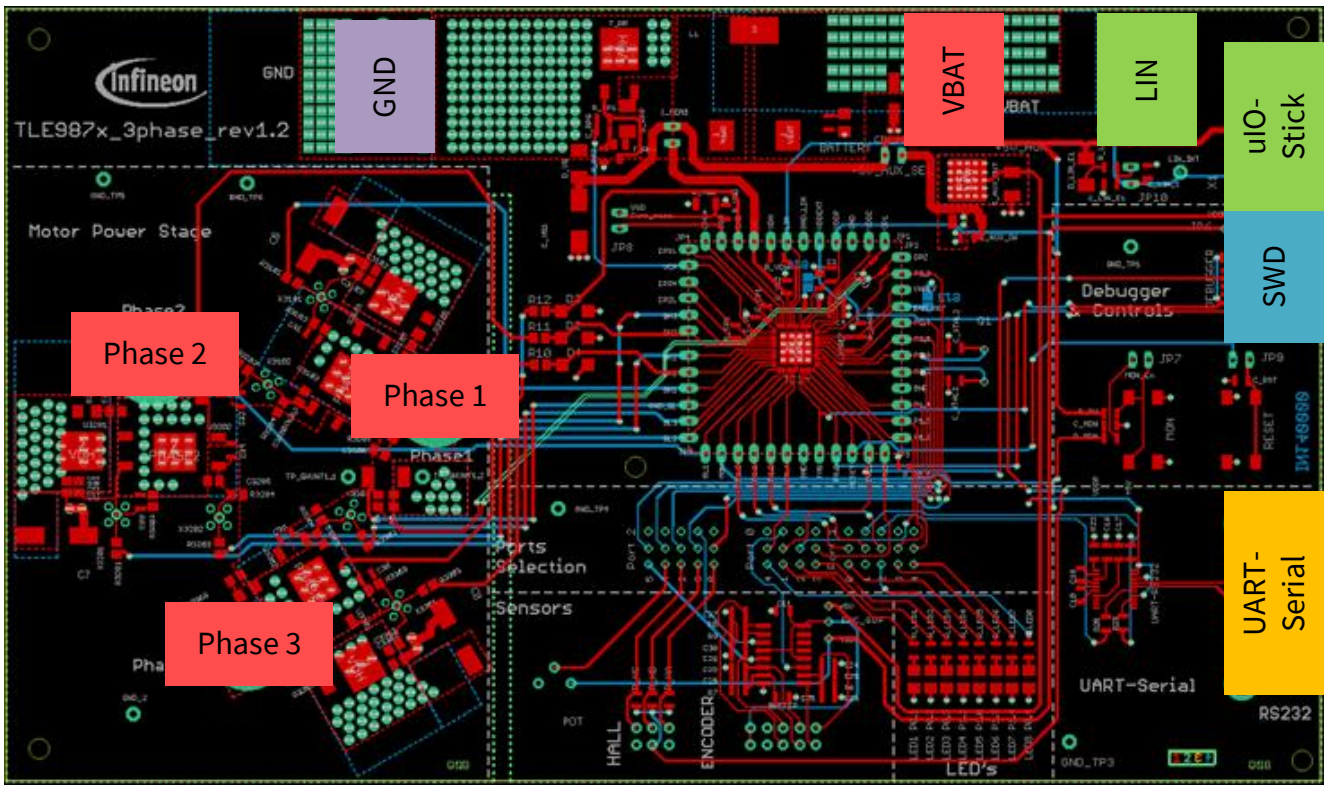

Figure 2 Interconnects

Banana jacks for ground, supply and LIN

There are jacks in different colors for ground, supply (max. 28 V) and LIN communication via banana jack. The following jacks are available: GND (marked purple), VBAT (marked red) and LIN (marked green).

Terminal pins for motor connection (marked red)

The three pins Phase1, Phase 2 and Phase3 provide access to the three half bridges and are intended to connect a brushless motor.

uIO Stick connector (marked green)

This uIO bootstrap loader is a 16-pin header (2 x 8) with 2.54 mm pitch.

It is intended to connect additional hardware for bootstrap loading. This interface can be used to programming the TLE987x via LIN (see **www.infineon.com/uio** or **www.hitex.com/uio**).

Interconnects

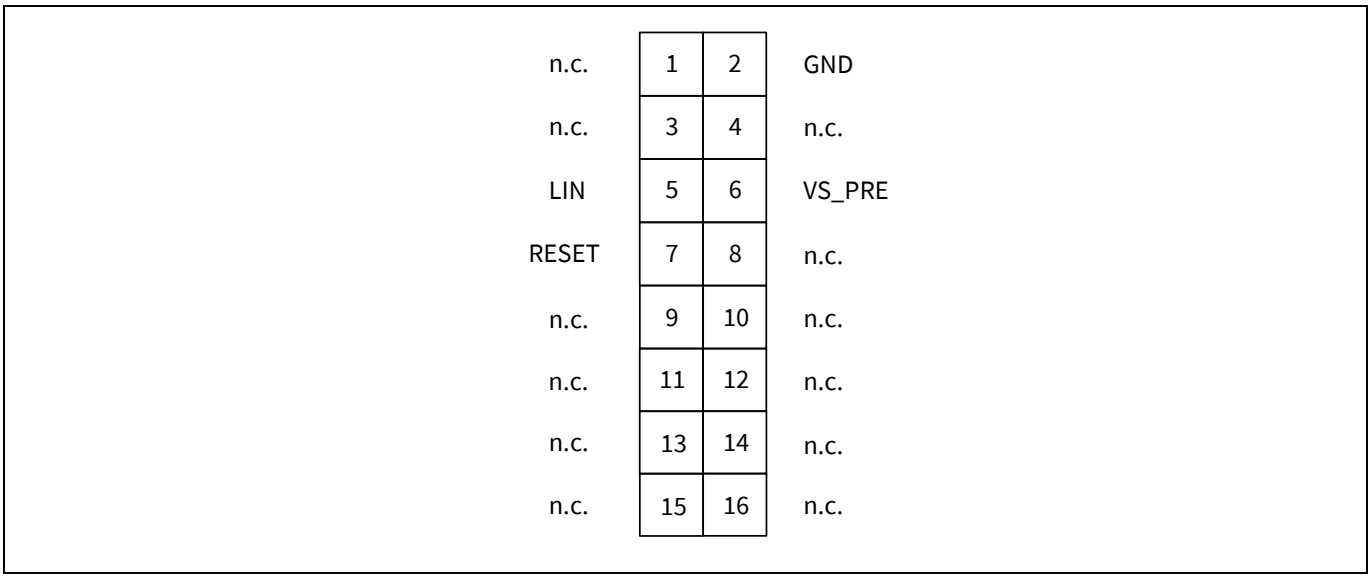

Figure 3 Pin configuration uIO BSL

Pin header for SWD (marked blue)

There is a 10 pin header (2 x 5) with 1.27 mm pitch on the evaluation board. This interface is meant to be used for debugging.

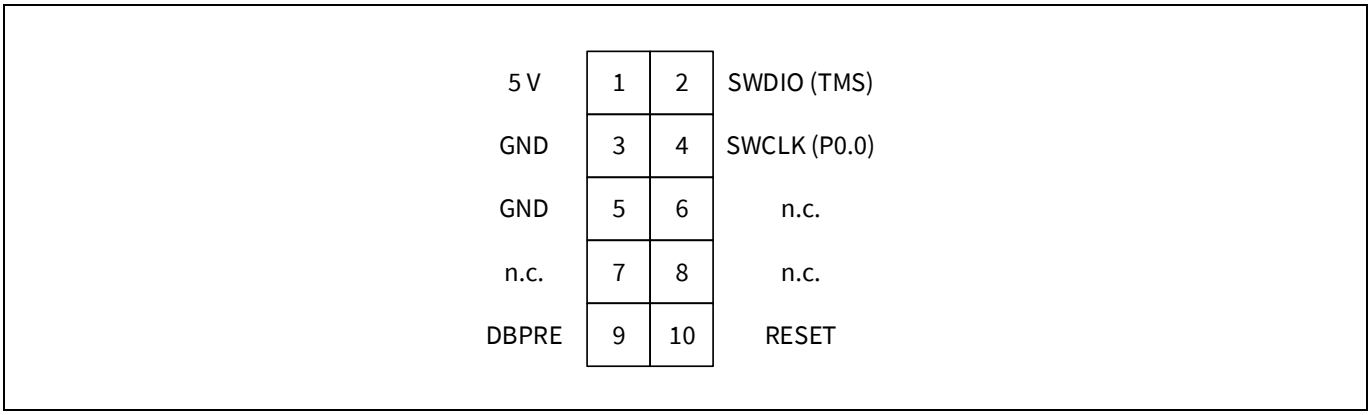

Figure 4 Pin configuration SWD interface

3 Test points and LEDs

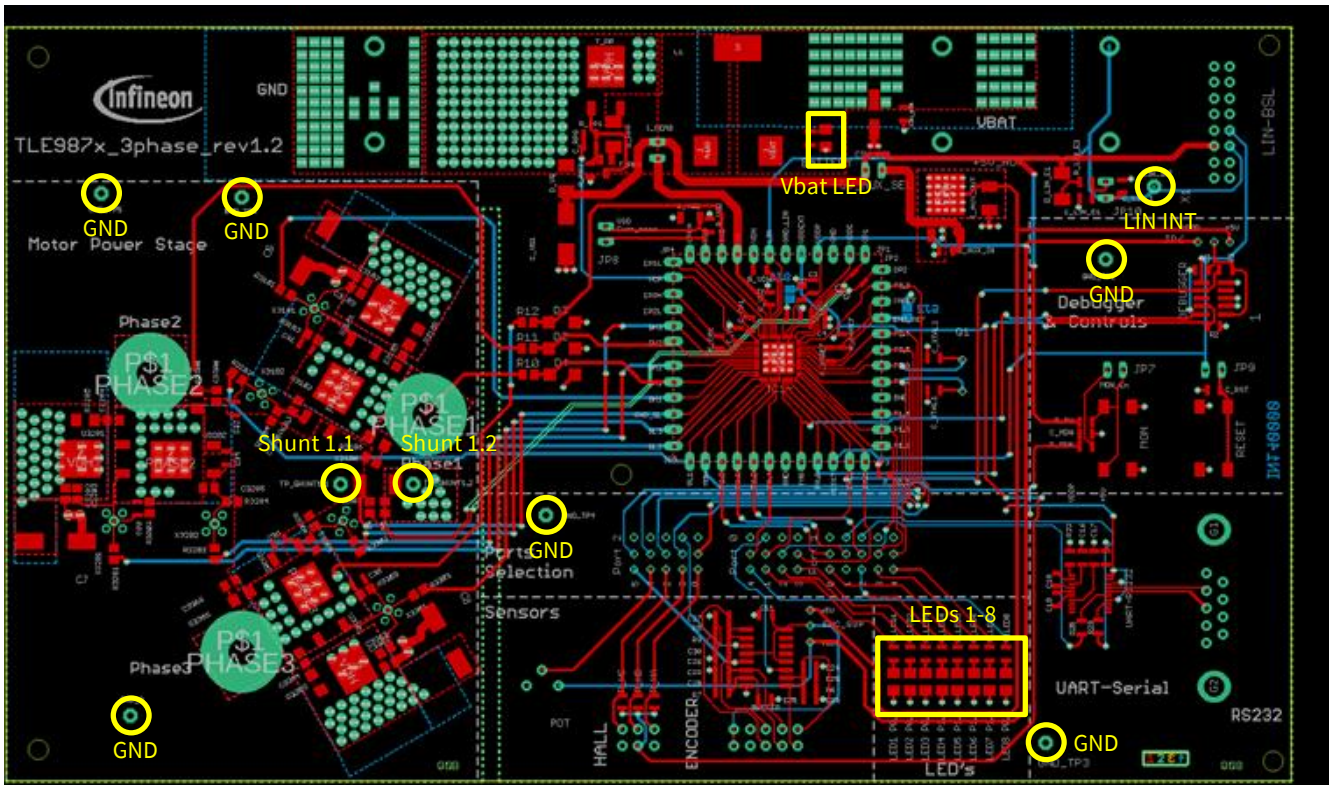

Figure 5 Test points

Several ground test points are provided.

Test points Shunt 1.1 and Shunt 1.2 are provided at both sides of the shunt, which is 5 mR.

Test point LIN_INT is used to measure the LIN voltage.

There are 9 LEDs for visual validations on the board:

- LED 1 to 8 can be connected to GPIOs (see **Table 3**).
- LED 9 (Vbat LED) indicates power supply.

4 Jumper settings

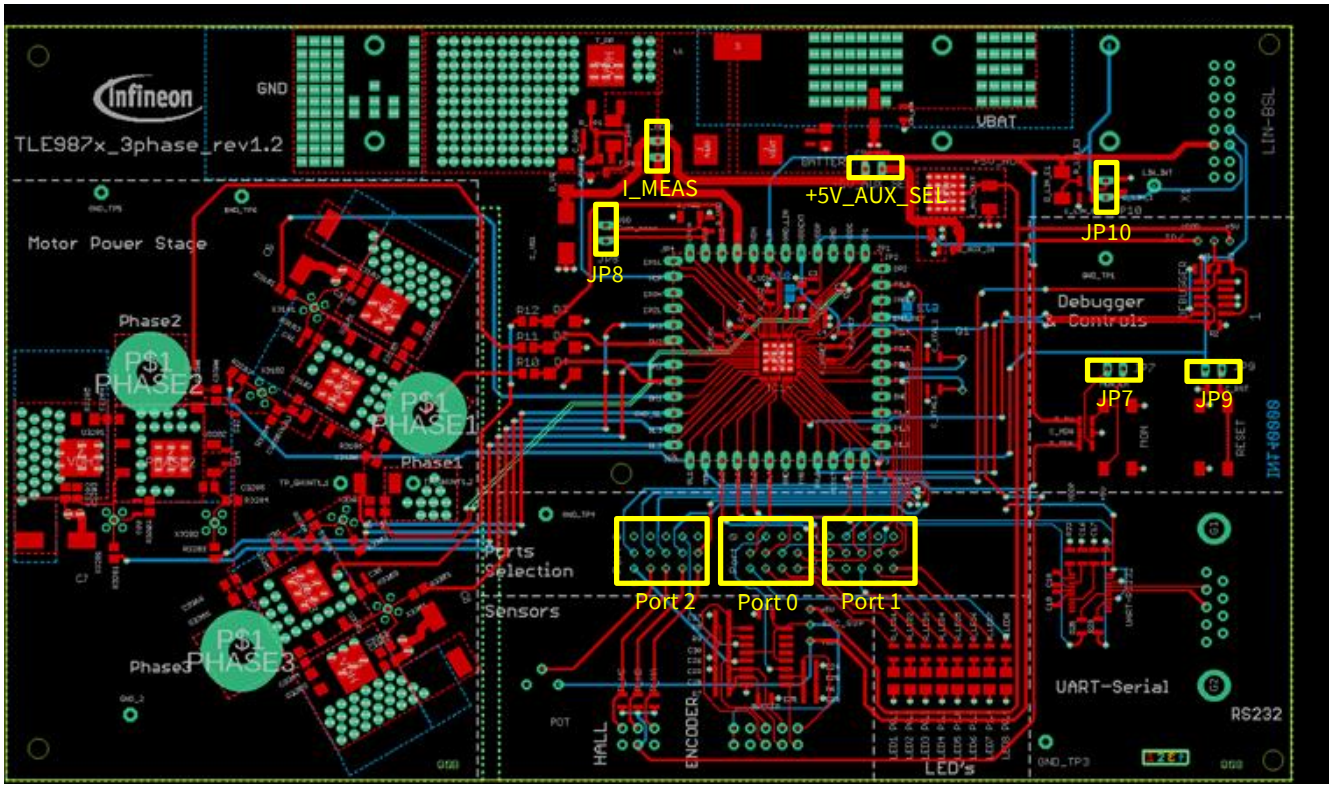

Figure 6 Jumpers

Table 2 Jumpers

JP7	Close this jumper to connect MON button to MON input. Open it to disconnect MON button from MON input.
JP8	This jumper is closed by default. If this jumper is left open the device is not supplied. It is intended to open the VS line in order to measure the current flowing into the TLE987x device.
JP9	Close this jumper to connect RESET button to RESET input. Open it to disconnect RESET button from RESET input.
JP10	Close this jumper to connect an additional 1 kΩ pull-up resistor. This is intended for LIN master communication. Open the jumper to use the TLE987x as slave in a LIN network. Software for LIN low level driver can be found at the homepage of IHR (**www.ihr.de**).
I_MEAS	This jumper is closed by default. If this jumper is left open the device is not supplied. It is intended to open the VSD line in order to measure the current flowing into the TLE987x device.
+5V_AUX_SEL	Open this jumper to disable the board's voltage regulator.
PORT 0/1/2	These jumpers can be put in two different positions (see **Figure 7**). Change these jumpers positon to connect or disconnect the LEDs, the potentiometer, the encoder or the Hall sensor (see **Table 3**).

Jumper settings

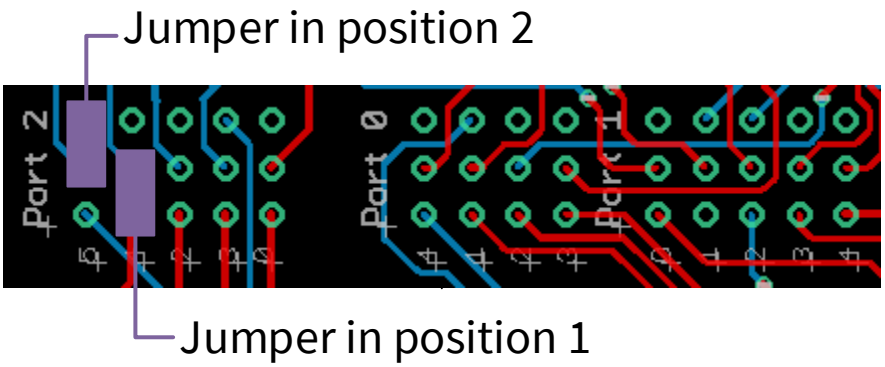

Figure 7 Jumper position

Table 3 GPIOs' function

Port	Position 1	Position 2
P0.1	LED 1	Encoder
P0.2	LED 2	/
P0.3	LED 3	/
P0.4	LED 8	/
P1.0	LED 5	/
P1.1	/	UART
P1.2	LED 4	UART
P1.3	LED 6	/
P1.4	LED 7	/
P2.0	Hall A	/
P2.4	POTI	/
P2.2	Hall C	/
P2.3	Hall B	Encoder
P2.5	Encoder	/

5 Communication interfaces

5.1 LIN (via banana jack and uIO BSL)

The device integrated LIN transceiver is connected to a banana jack and additionally to the uIO BSL interface. To integrate the device in a LIN network it is sufficient to use the single wire banana interface. The BSL interface is intended to program the device via LIN. For further information about the uIO interface see **www.infineon.com/uio** or **www.hitex.com/uio**.

5.2 UART

A RS232 connector on the board enables a serial communication.

5.3 Debugging

Debugging is possible via the SWD interface; the signals are routed through the 10 pin header SWD interface The pin configuration makes sure that the XMC is hold in reset while another debugger is physically connected as DBPRE will be implicitly connected to GND by connecting the external ISP (see **Figure 4**).

6 Software toolchain

6.1 Keil µVision 5

The recommended Integrated Software Development Environment is Keil® µVision5®.

Infineon's Embedded Power family is supported. For more information about the installation process, go to **www.keil.com**.

6.2 Infineon ConfigWizard

In addition to the IDE, Infineon provides a solution to speed-up the IC programming, the "ConfigWizard". This tool is designed for code configuration in combination with the IDE. Infineon ConfigWizard can be downloaded via the Infineon Toolbox. The Infineon Toolbox is a central place to download and update all your Infineon tools. It can be downloaded from **www.infineon.com/toolbox**.

6.3 TLE987x SDK

All Embedded Power products can be installed to Keil® µVision5® via "Pack Installer". Browsing to the Infineon chapter in "All Devices" will lead to the "TLE98xx Series". The ".pack" file comes with several code examples to provide an easy start up and speed up software development.

6.4 Debug connection setup

For a proper Flash and Debug Connection, install V5.10 (or newer) from: **www.segger.com/jlink-software.html**. Keil® µVision5® has to be configured in the IDE Menu "Options for Target". After connecting the USB-cable and power up the EvalBoard, go to the "Debug" register-card, choose "J-LINK / J-TRACE Cortex" and press "Settings".

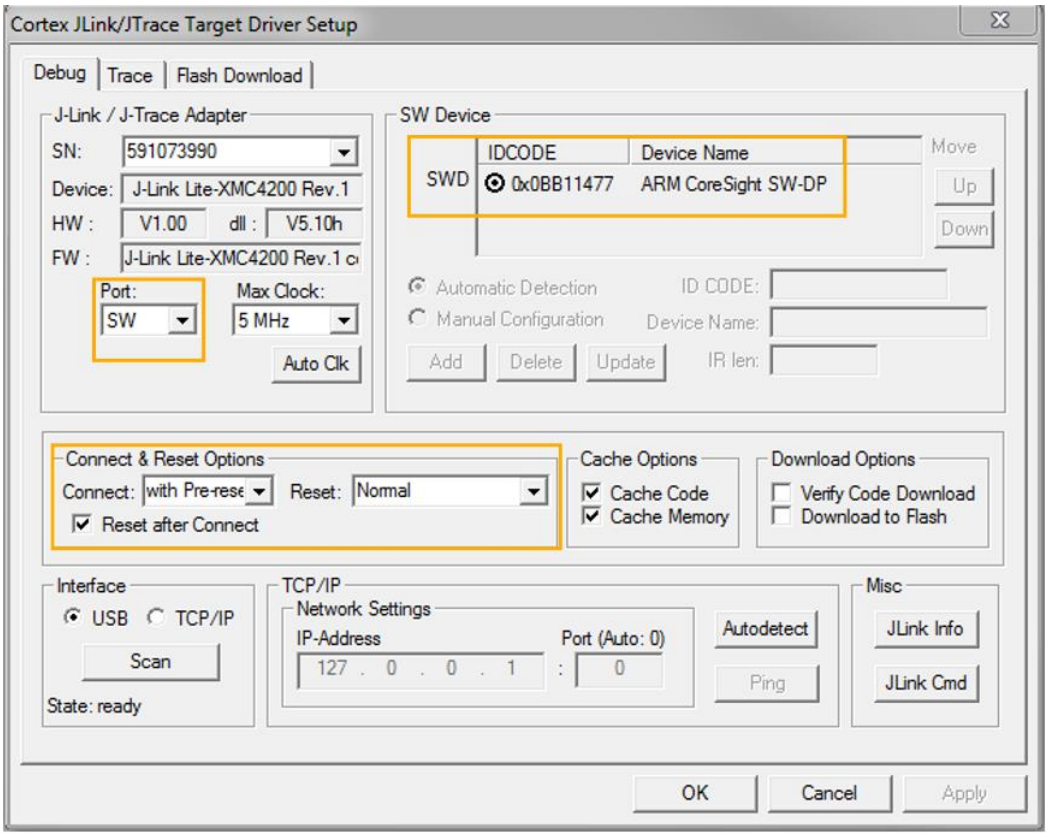

Figure 8 Debug and flash configuration

If the board is connected successfully, the Arm® IDCODE will be visible in the SW Device Window. If connection fails, “Connect & Reset Options” and “Port” window has to be checked.

7 Technical data

Table 4 Technical data

Voltage supply:	max. 28 V
Motor current:	max. 20 A
Pin ports:	5 V

8 Optional additional placements

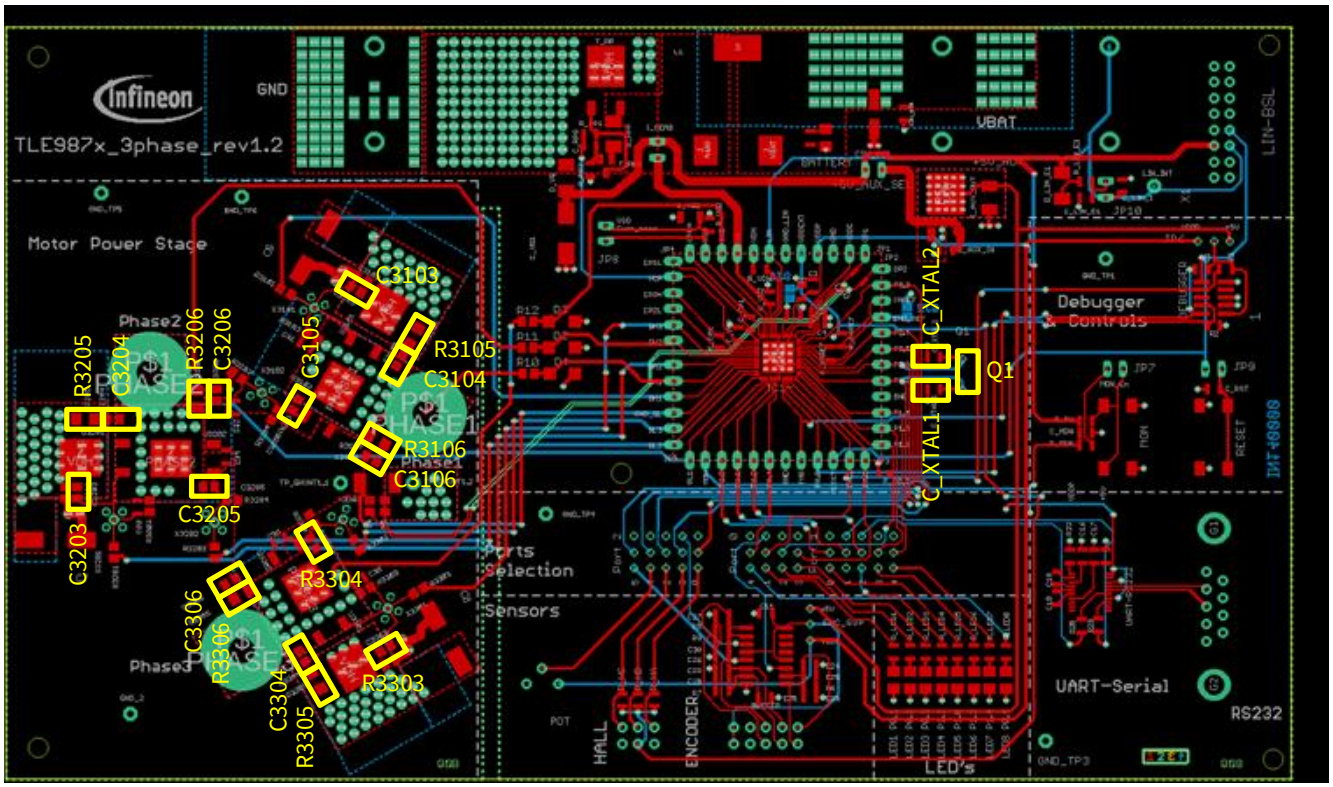

Figure 9 Additional placements' positions

Values for these optional additional placements have to be determined depending on application.

Table 5 Additional placements

Component	Description
Q1	External oscillator
C_XTAL1	Oscillator capacitor 1
C_XTAL2	Oscillator capacitor 2
R3105	Resistance snubber high-side MOSFET phase 1
C3104	Capacitor snubber high-side MOSFET phase 1
C3103	Gate drain capacitor high-side MOSFET phase 1
R3106	Resistance snubber low-side MOSFET phase 1
C3106	Capacitor snubber low-side MOSFET phase 1
C3105	Gate drain capacitor low-side MOSFET phase 1
R3205	Resistance snubber high-side MOSFET phase 2
C3204	Capacitor snubber high-side MOSFET phase 2
C3203	Gate drain capacitor high-side MOSFET phase 2
R3206	Resistance snubber low-side MOSFET phase 2

Optional additional placements

Component	Description
C3206	Capacitor snubber low-side MOSFET phase 2
C3205	Gate drain capacitor low-side MOSFET phase2
R3305	Resistance snubber high-side MOSFET phase 3
C3304	Capacitor snubber high-side MOSFET phase 3
C3303	Gate drain capacitor high-side MOSFET phase 3
R3306	Resistance snubber low-side MOSFET phase 3
C3306	Capacitor snubber low-side MOSFET phase 3
C3305	Gate drain capacitor low-side MOSFET phase 3

9 Schematics and layout

9.1 Schematic

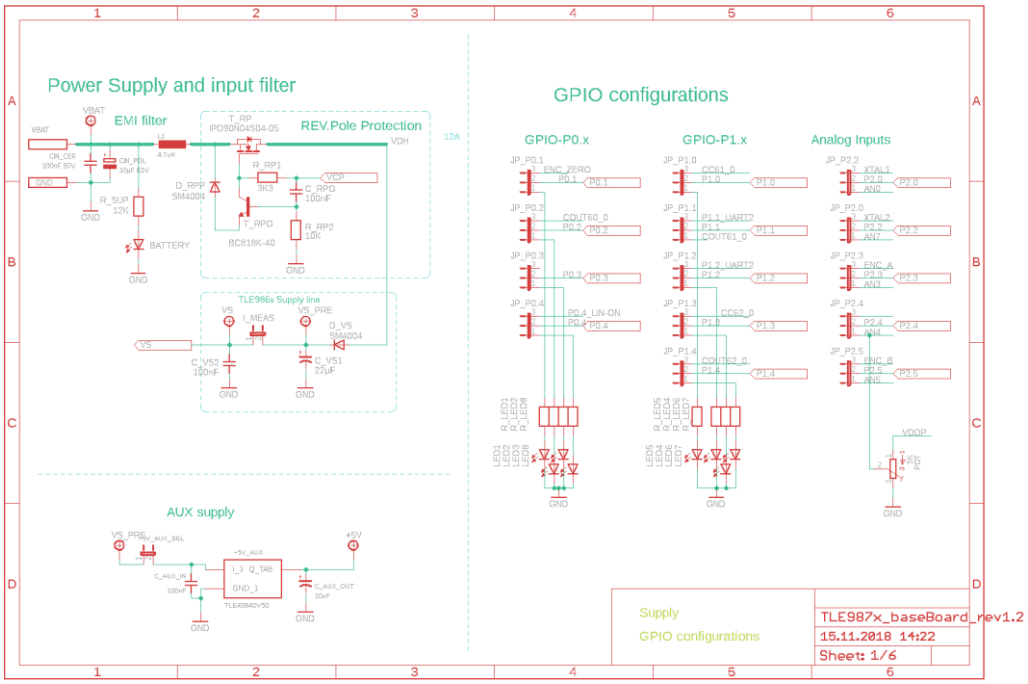

Figure 10 Schematics: Sheet 1

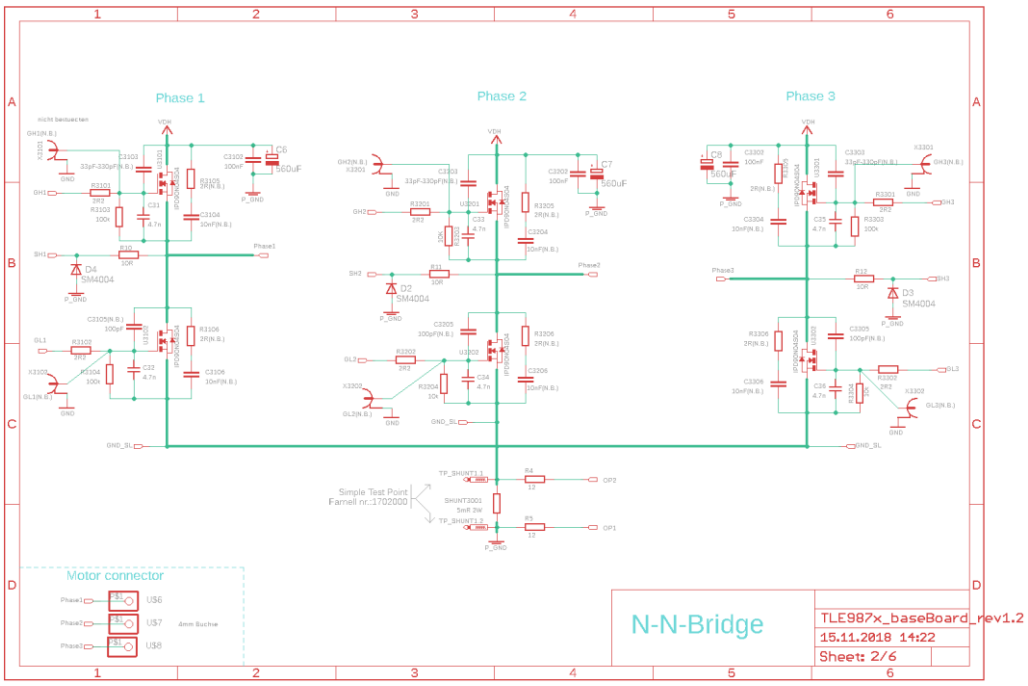

Figure 11 Schematics: Sheet 2

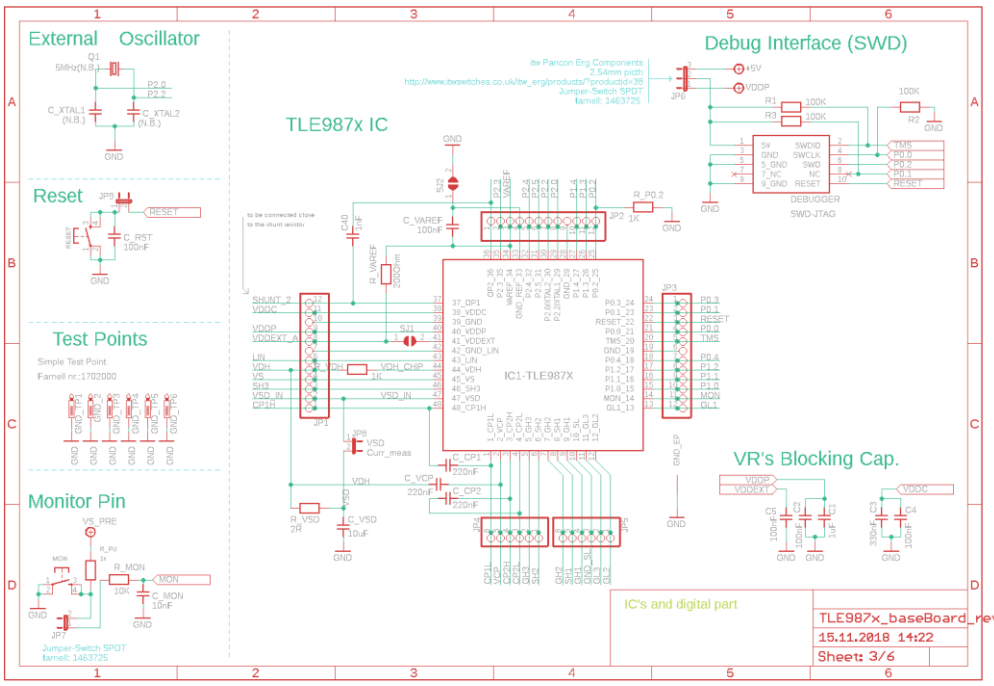

Figure 12 Schematics: Sheet 3

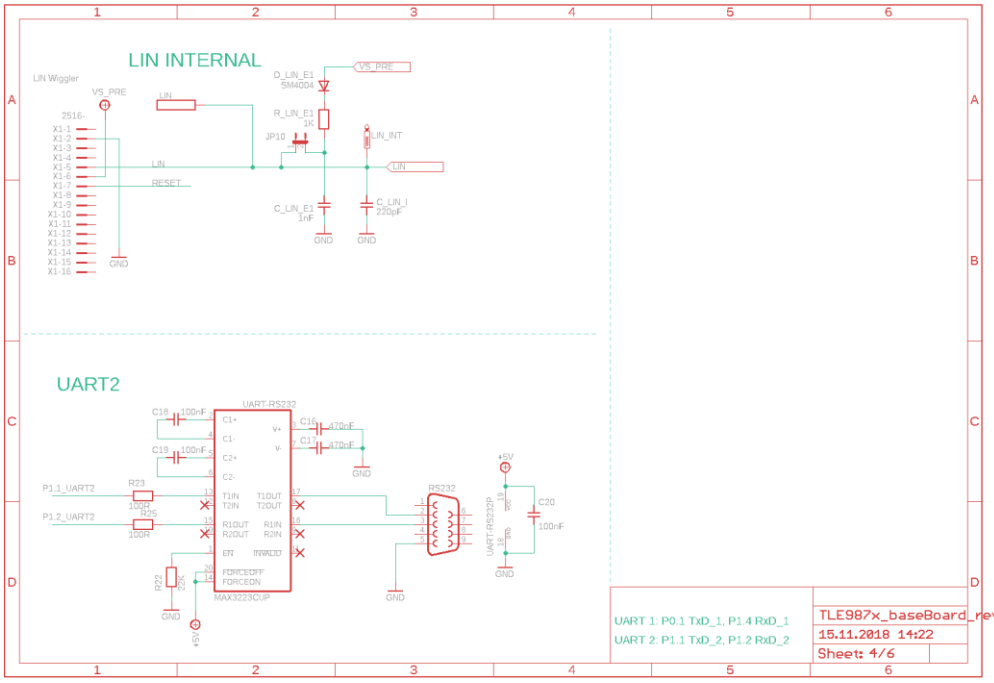

Figure 13 Schematics: Sheet 4

Schematics and layout

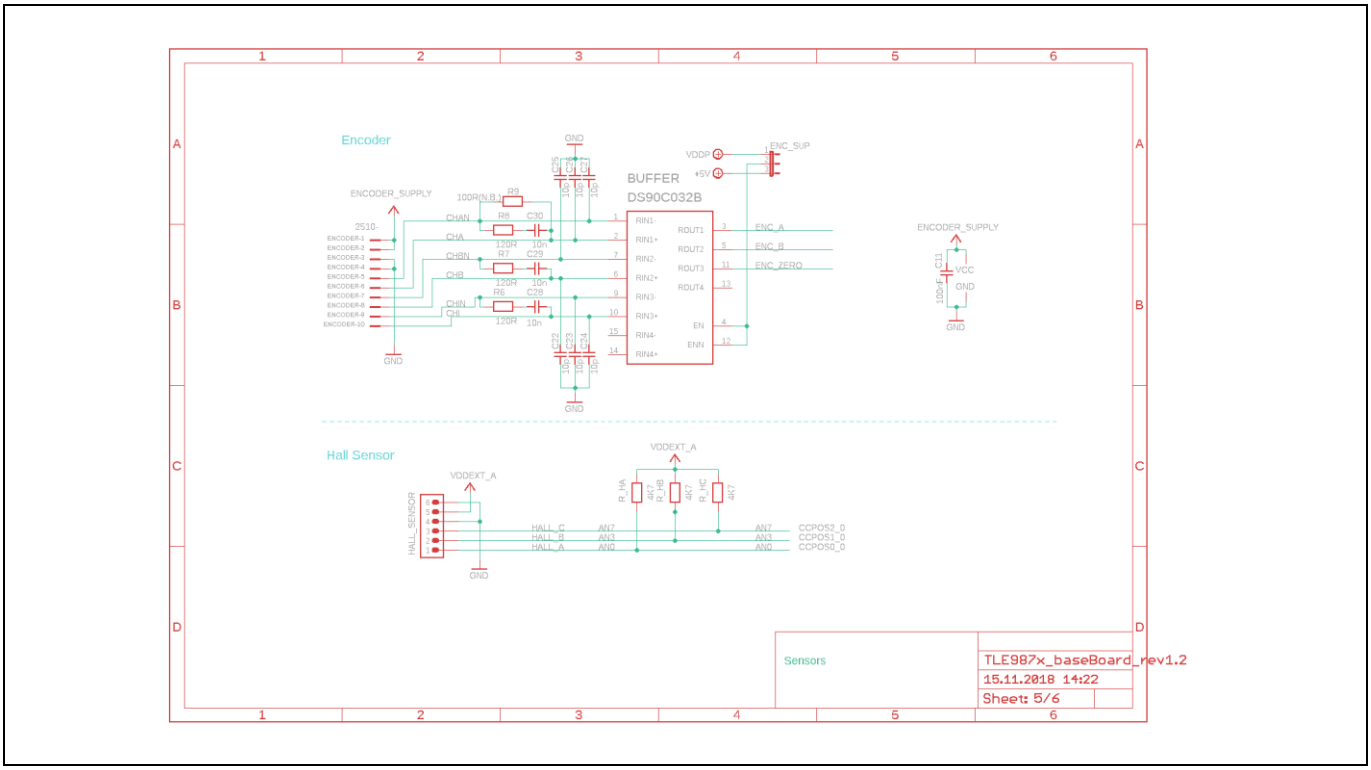

Figure 14 Schematics: Sheet 5

9.2 Layout

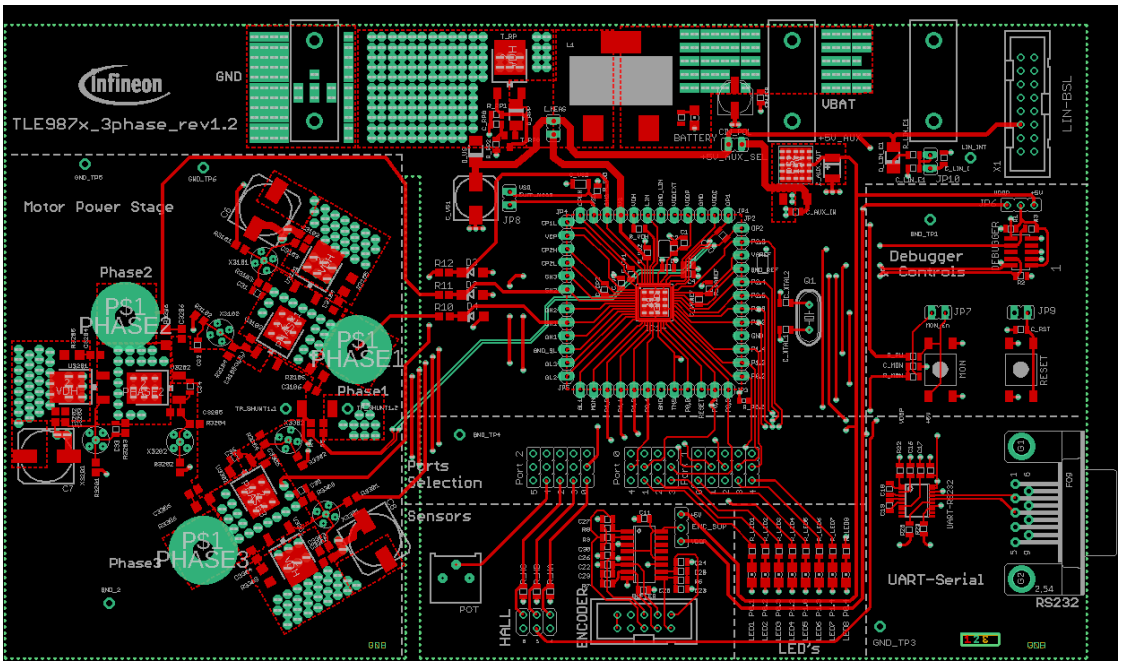

Figure 15 Top layer

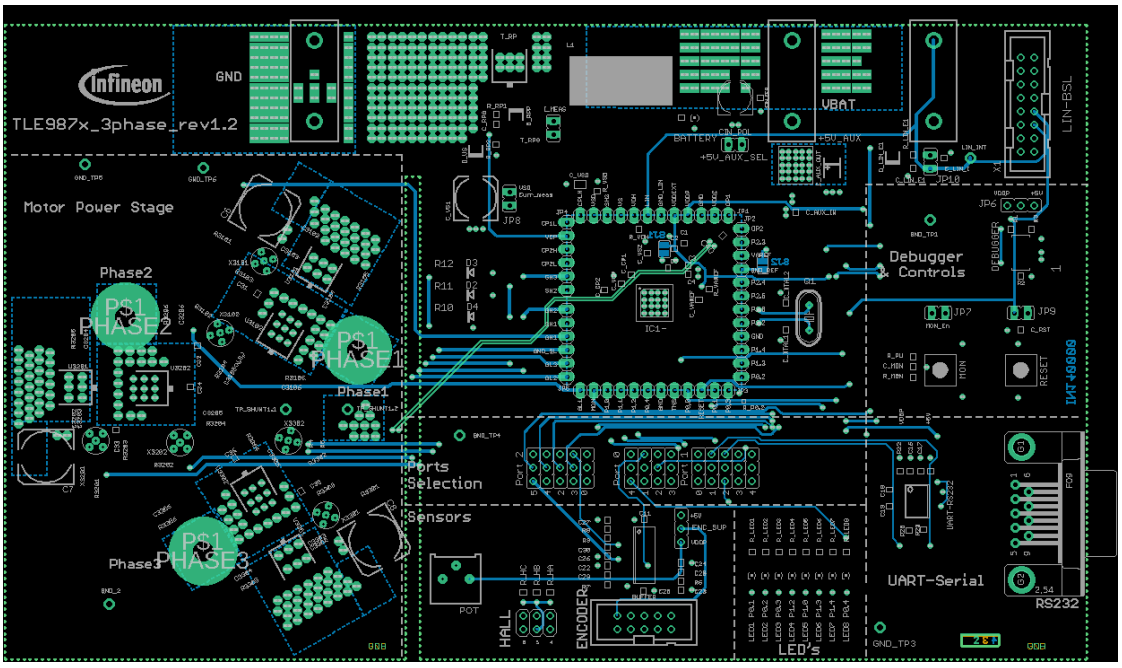

Figure 16 Bottom layer

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